EECT 6326

Analog Integrated Circuit Design

Design of a Two Stage Amplifier

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Contents

1. Design Specifications

Design a differential input and single-ended output amplifier. The amplifier is to be powered from a 1.5 V power supply. The amplifier has only one ideal current source, ISS. Use IBM 0.13 μm CMOS process to best meet the following specifications:

Specifications	Required	Obtained
Supply Voltage, (VDD)	= 1.5 V	1.5 V
Capacitive Load, (CL)	= 2pF	2pF
Output Voltage Swing Range (OVSR)	>1.20V	1.217
Voltage Gain, (Avd = vo/vid)	≥ 75 dB	76.9608dB
Unity-gain frequency, (UGF)	≥ 5 MHz	6.91MHz
Phase margin, (PM)	≥ 60 °	61.197
Total Power Dissipation, (Pdiss)	≤ 0.1mW	0.087405mW
Common mode rejection Ratio (CMRR)	> 70dB	70.8598db
Average Slew Rate (Sr+ + Sr-)/2	>4 V/us	5.65V/us

Figure 1. Table of Design specifications

2. Introduction

Our approach to designing the circuit was inspired from the two stage amplifier chapter in the Razavi textbook. We simulated the performance of the differential amplifier topology.

3. Design Considerations

In our circuit we have used the following W/L ratios for the transistors –

- (W/L) M1 = (W/L) M2
- (W/L) M3 = (W/L) M4 = 3x (W/L) M1,2
- (W/L) MB0
- (W/L) MB2

4. Hand Calculations

Power Dissipation = Vdd * (Current through all branches in the circuit)

Pdiss ≤ 0.05mW

VDD * ISS ≤ 0.1 mW

I ≤ (0.1 *10^-3 / 1.5)

I ≤ 66 μA   My power budget for my current mirrors

Unity Gain Frequency

Fu ≥ 5MHz
Wu = 2*pi*Fu
Wu ≥ 2*pi*5MHz
Wu ≥ 10*pi Mhz = pi*10^7
Wu ≥ 3.15*10^7 or 31.5 rad/s This means Avd =0 must occur beyond 31.5rad/s

<u>Small Signal</u>

For Phase margin ≥ 60 °
P2=2*UGF => Gm2/CL = 2 *Gm1/Cm = 2 (5.3MHZ) (2pi)
Gm2 = (10.6M)*(2pi) (2pF)= 133.3uA/V → target
Gm1 = 150uA/V → original assumption

Cm = 2*Gm1/Gm2 *CL* = 2150/133.2(2pF) = 4.5pF = Cm
Rm = 1/Gm2 = 1/133.2u = 7.5Kohms = Rm
Assume R1= 1.5Mohm
If Gain with a margin = 75db+3db =78dB = 7943028
RL = Gain/(Gm1*Gm2*R1) = 7943.28/(133.2u *150u * 1.5M) = 2650.041Kohm

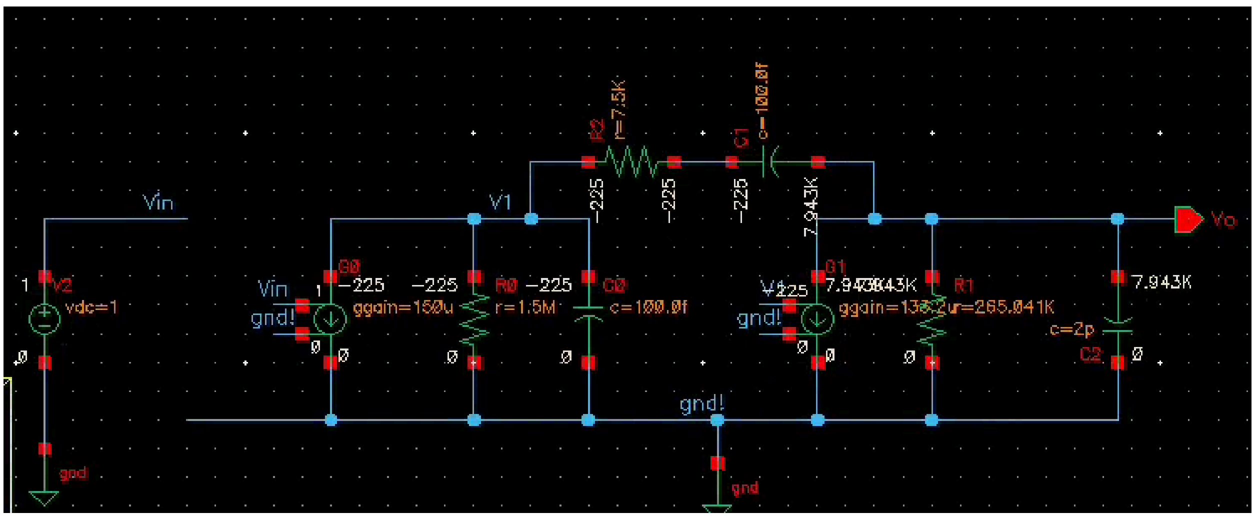

Figure 2. Small Signal model gain check w/ parameters

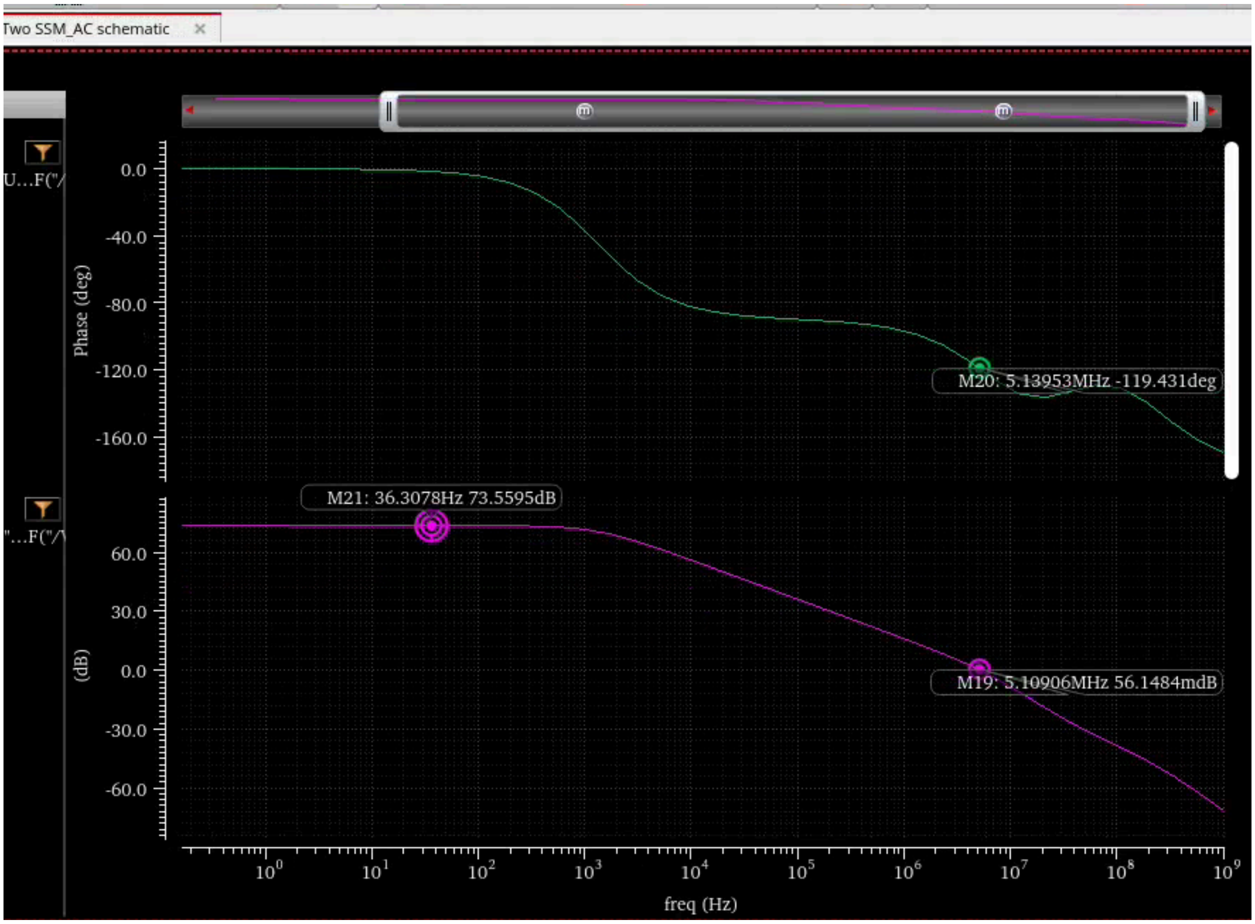

Figure 3. Small signal ac stability check

<u>1st Stage design.</u>

Finding out how to tweak a small signal model for desired effects.

Gm1 =175uA/V

IB0 > SR * Cm = 4.2 V/us *4.5pF = 18.9uA

Assuming Lmin is =0.4um and we should do 4x the min we will do

L = 0.4um x 4 = 1.6um

W1,3 is set to 11.2um therefore W2,4 = 3* W1,3 = 3 *11.6um = 33.6um

And found 30uA bias allows for a Gm1 of 175. After, performed a quick ac test to see dc gain is 266 for first stage while >250 is desired

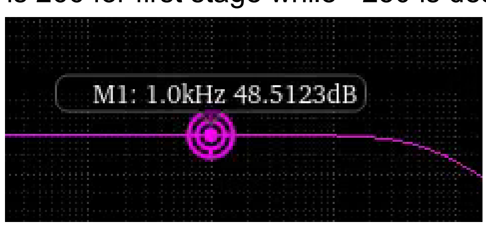

Figure 4. Avd 1st stage check

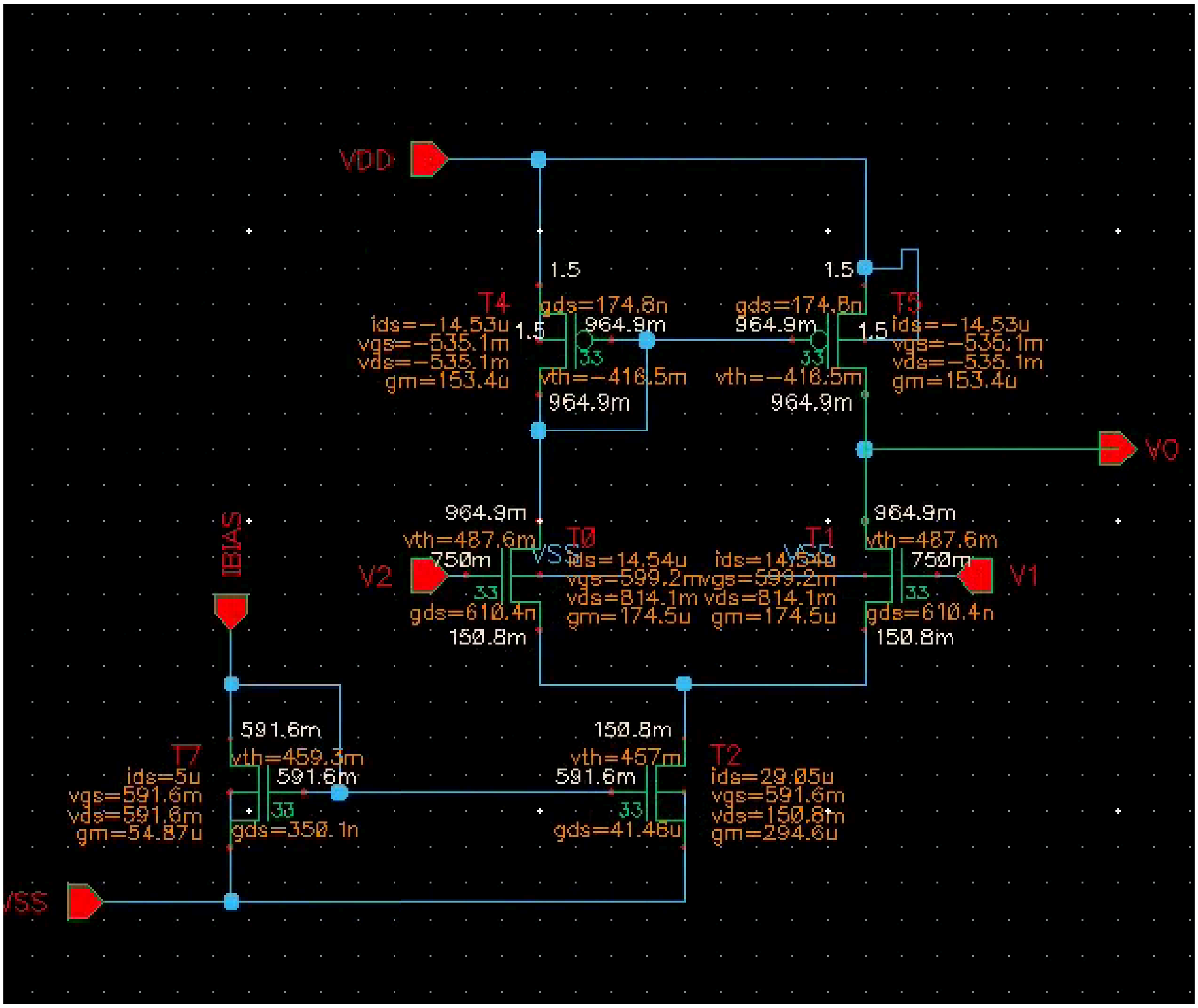

Figure 5. 1st stage amplifier schematic

Everything in saturation with dc check and gm 1,2 is 175 is good

<u>2nd Stage design</u>

Sizing W of ML is essential the IB2/ID3 *(W/L)3 so WL was tweaked after tests to be 67.2um which helps us find biasing currents within our bias current budget

Mb1 was original twice as big as M1,4 but when changes were made it was left at 19.2um and Mb0 was reduced to reduce overall power dissipation and then Mb2 was tweaked to achieve the right current to make sure the two stage amplifier was in saturation with the proper spec values

(Ib0+Ib1+Ib2) *VDD < 0.1mW

Ib0+Ib1+Ib2 < 66.66uA

I would find tweaking the second stage with the right parameters would change my Gm2 values and a bit of my Gm1 when I altered current. This changes my Cm and Rm values which end up being Cm = 4.5pF & Rm = 3.257K

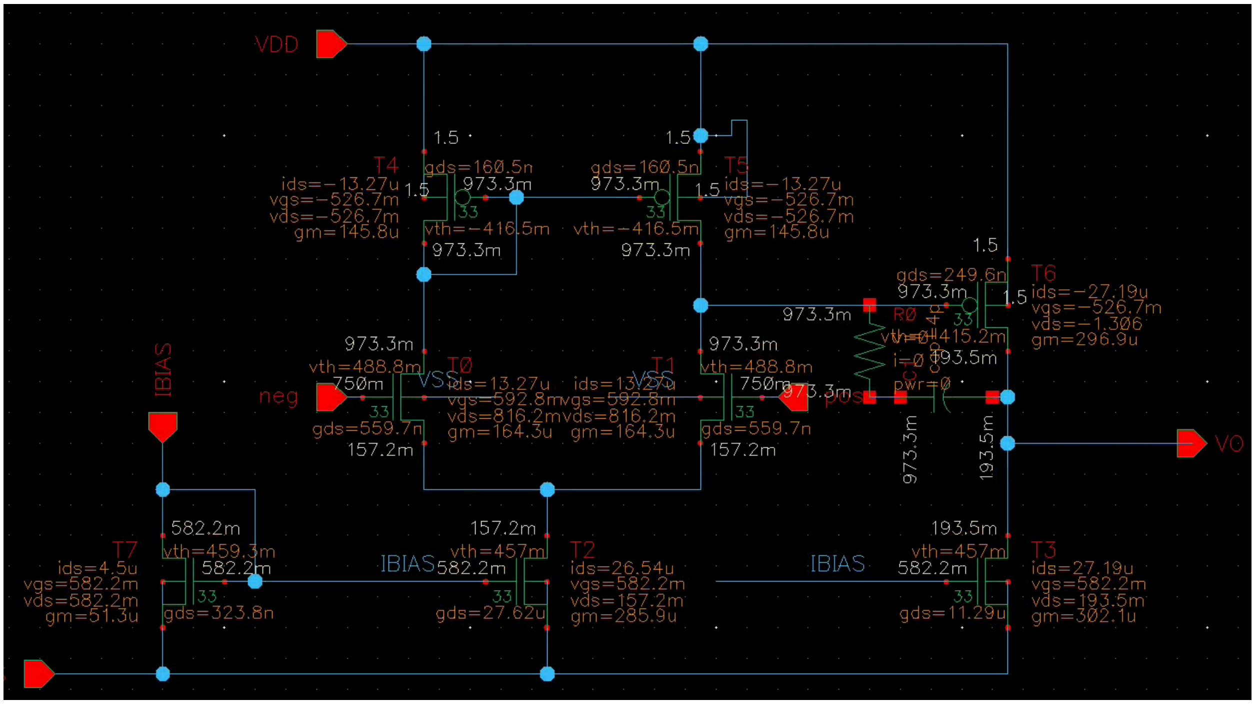

Figure 6. Two stage schematic saturation

5. Device sizing and biasing table

Transistors	W(μm)	L(μm)	W/L ratio	Ids(μA)
Mb0	4.8μm	1.6μm	3	4.5 uA
Mb1	19.2 μm	1.6μm	12	26.54 μA
Mb2	19.2 μm	1.6μm	12	27.19 μA
M1, M4	11.2μm	1.6μm	7	13.27 μA
M3, M2	33.6μm	1.6μm	21	13.27 μA
ML	67.2μm	1.6μm	42	27.19 μA

Figure 7. Table of W/L design of transistors

KEEP IN MIND MY VSS = 0 =GND

6. Schematics of the amplifier

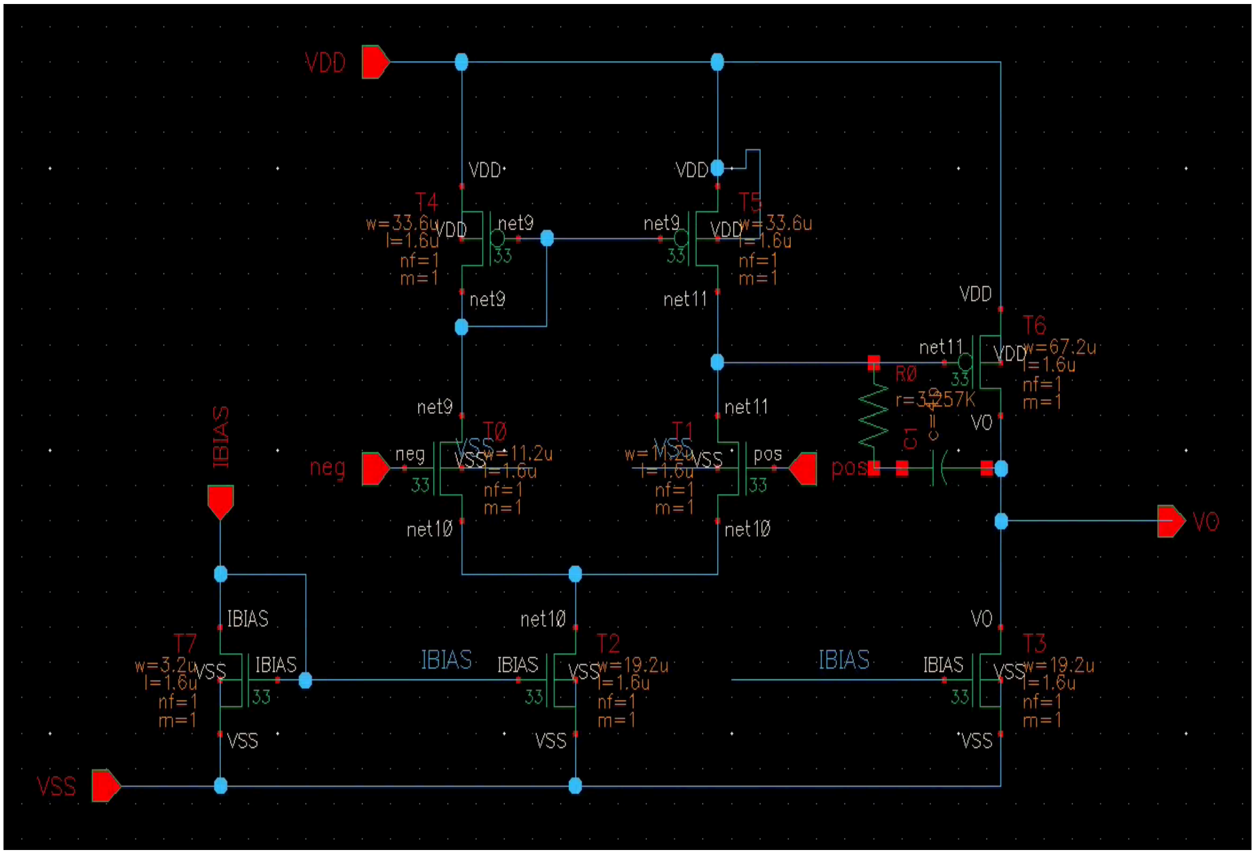

Figure 8. Schematic of Two Stage Amplifier

6.1 Symbol of Amplifier

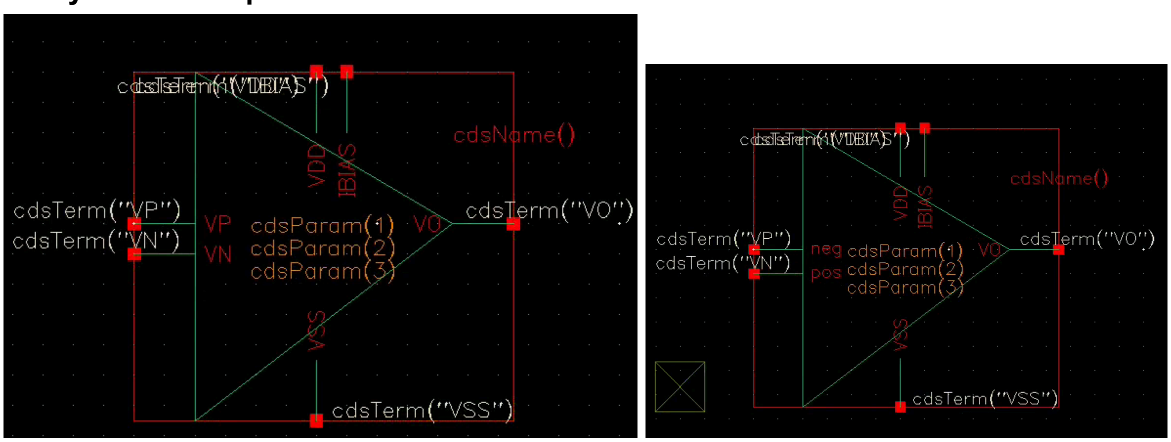

Figure 9. Symbol of amplifier

Sorry had pos and neg like that on the new tested symbol

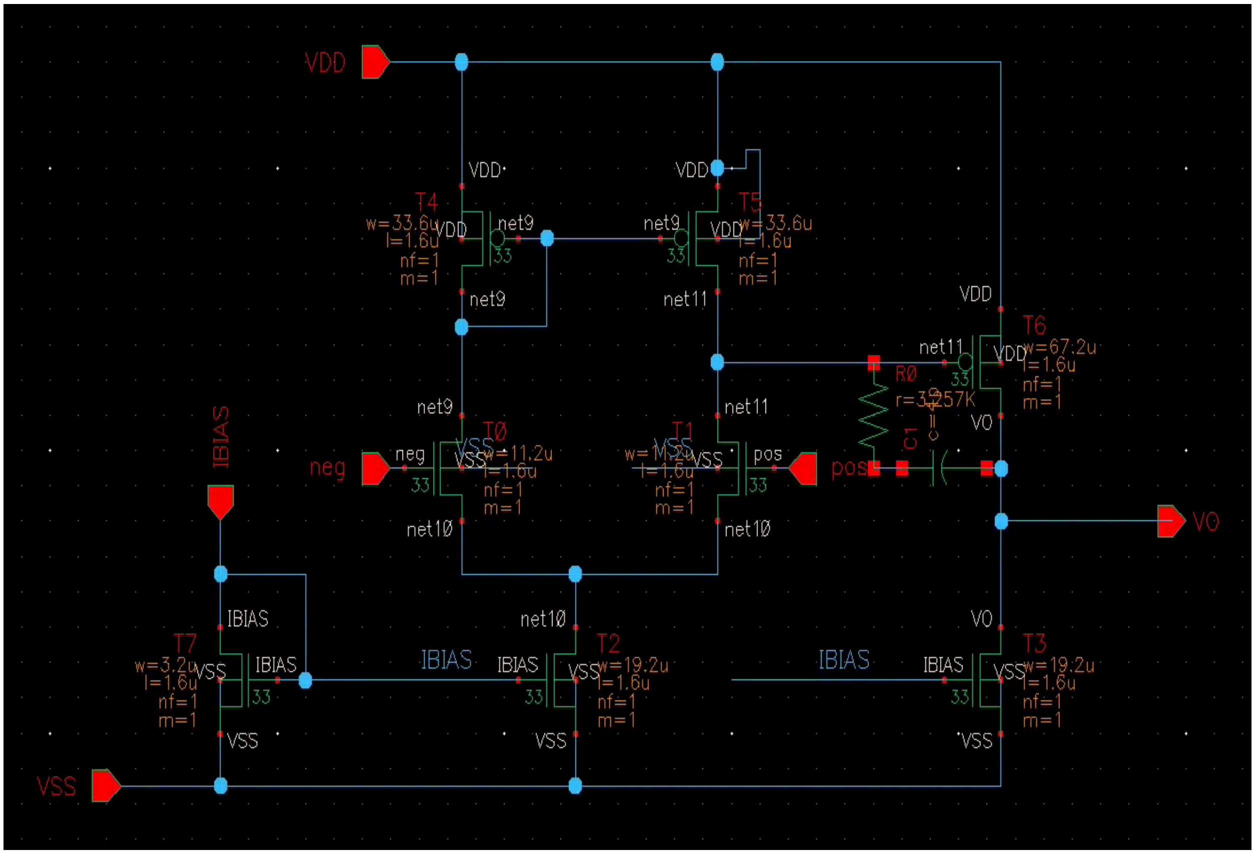

Figure 10. Two stage sizes and schematic used for tests

7. Results and Setups

7.1 OVSR

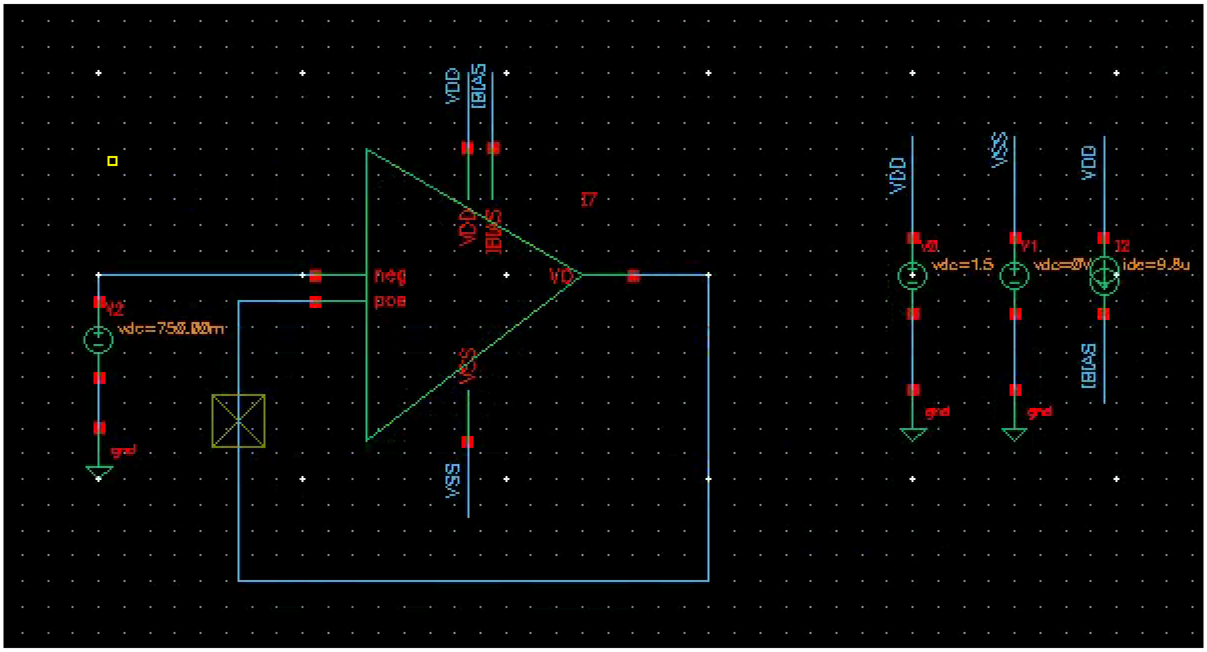

Figure 11. DC Test Schematic method 1

Figure 12. Output swing of method 1

swing 1.3877-0.116 +1.21717

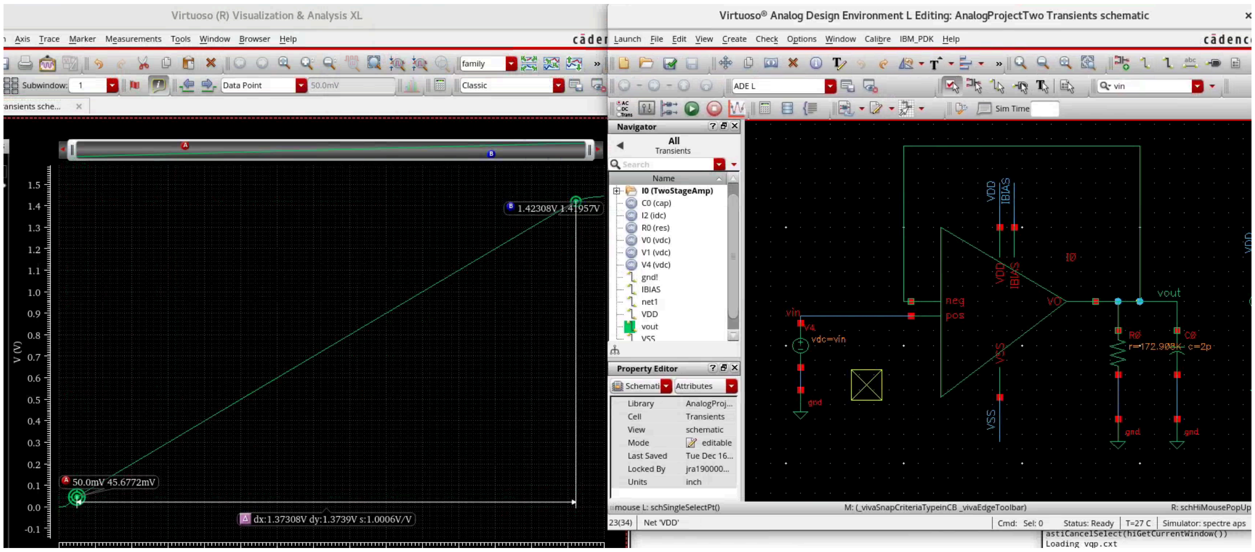

Figure 13. Output and Schematic of method 2

method two finding range of linear region

1.419 and 0.04567 = 1.3733 well I am going to use the other one b/c worse case… and it still obtain original goal anyways

7.2, 7.3, 7.4 GBW, Avd, PM

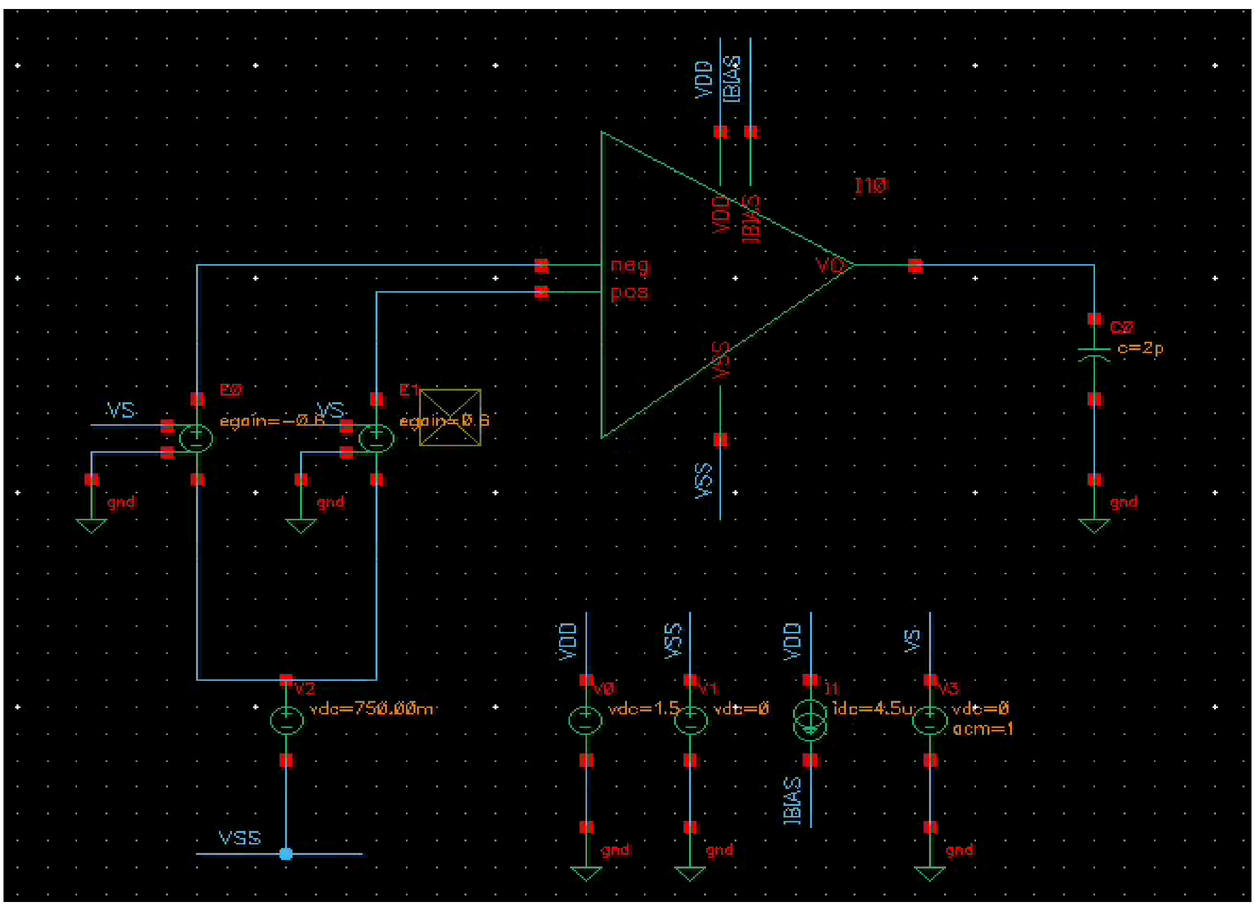

Figure 14. Schematic for Avd, GBW, PM tests and dc sweep

Figure 15. Frequency response output graph

UGB = 6.91 MHZ
Avd = 76.96 dB
PM = 180-118.803 = 61.197 degrees

power dissipation

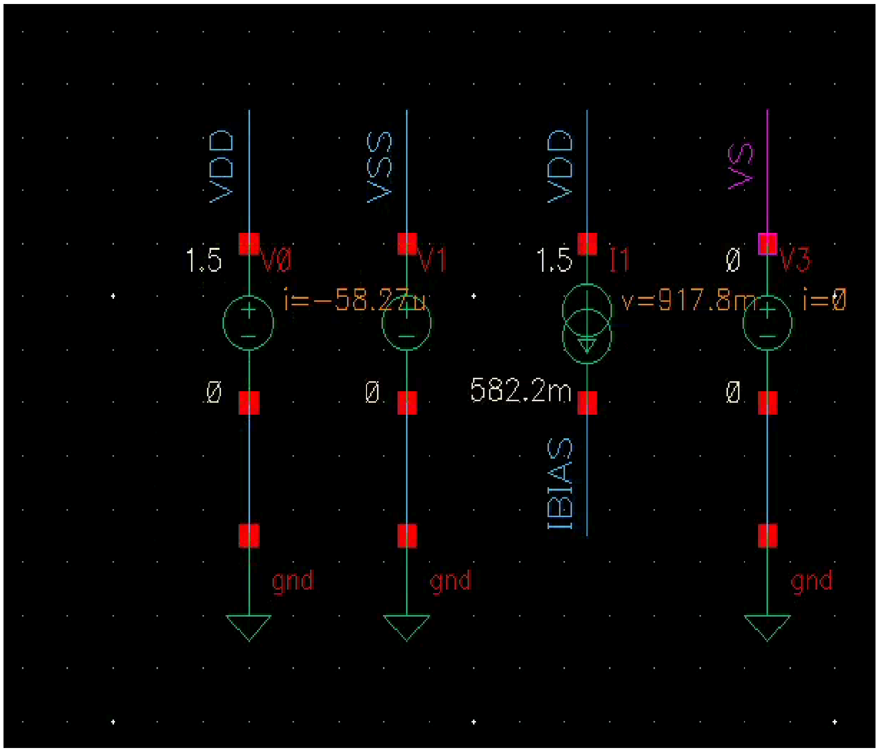

Figure 16. Current consumption

58.27*1.5=87.405uW or 0.087mW

CMRR

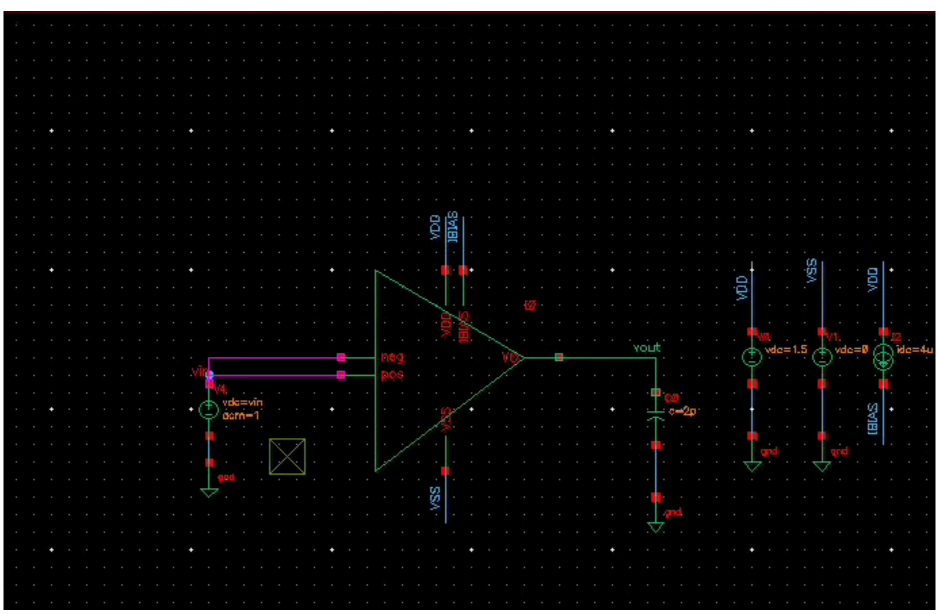

Figure 17. Schematic for CMRR tests

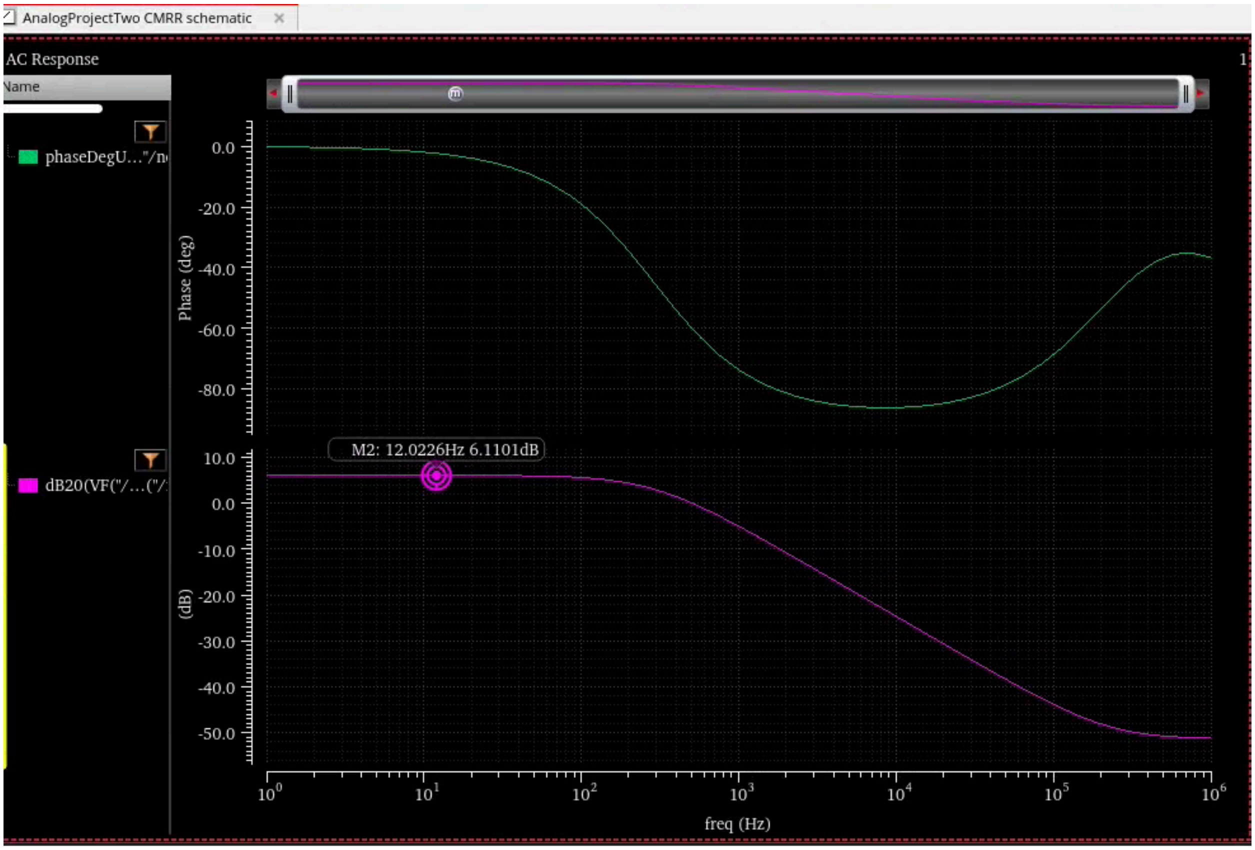

Figure 18. CMRR output

6.101db

76.9608-6.101 = 70.8598db = CMRR

Average Slew Rate

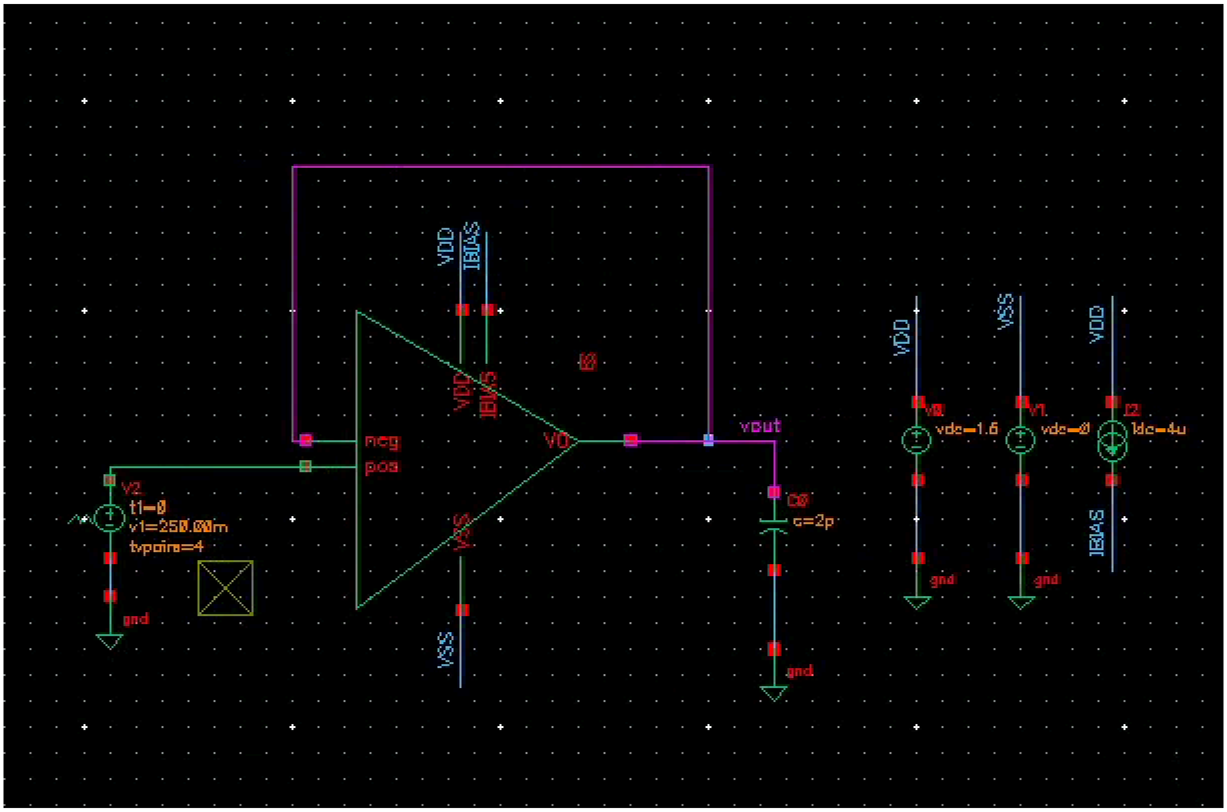

Figure 19. Schematic for transients

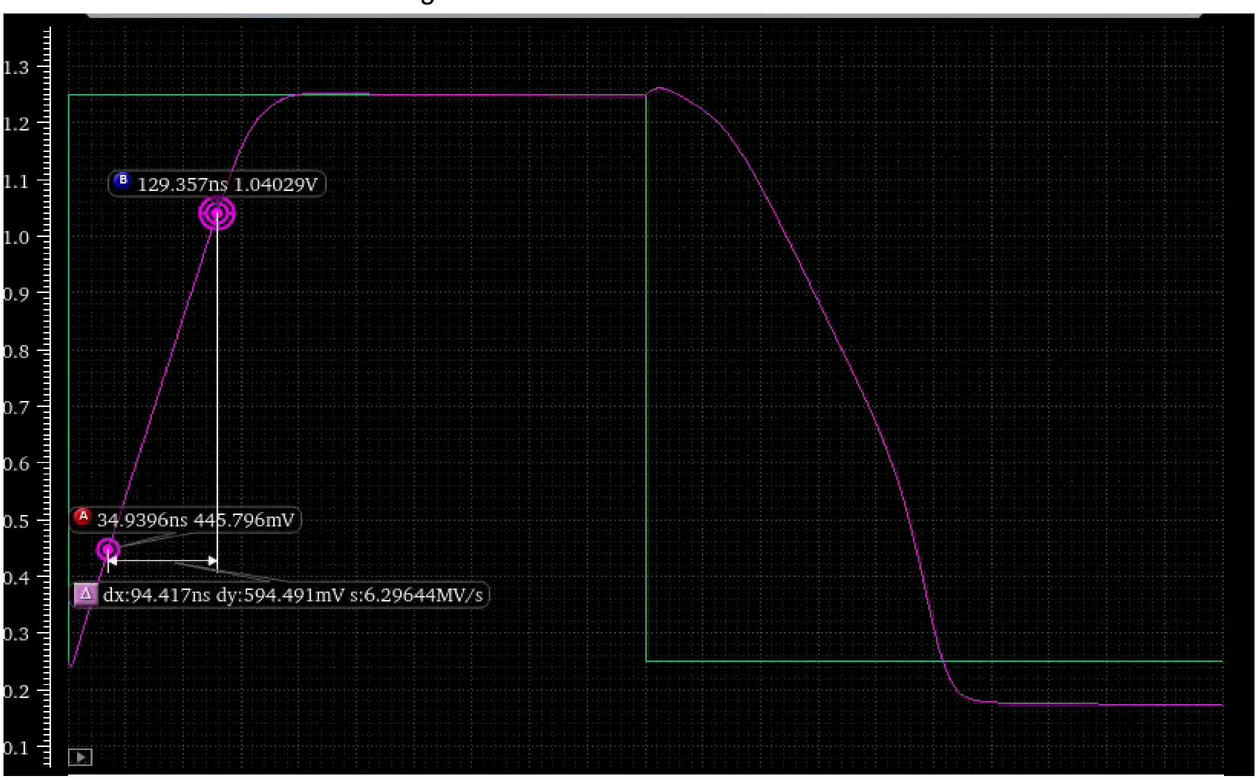

Figure 20. Transient response

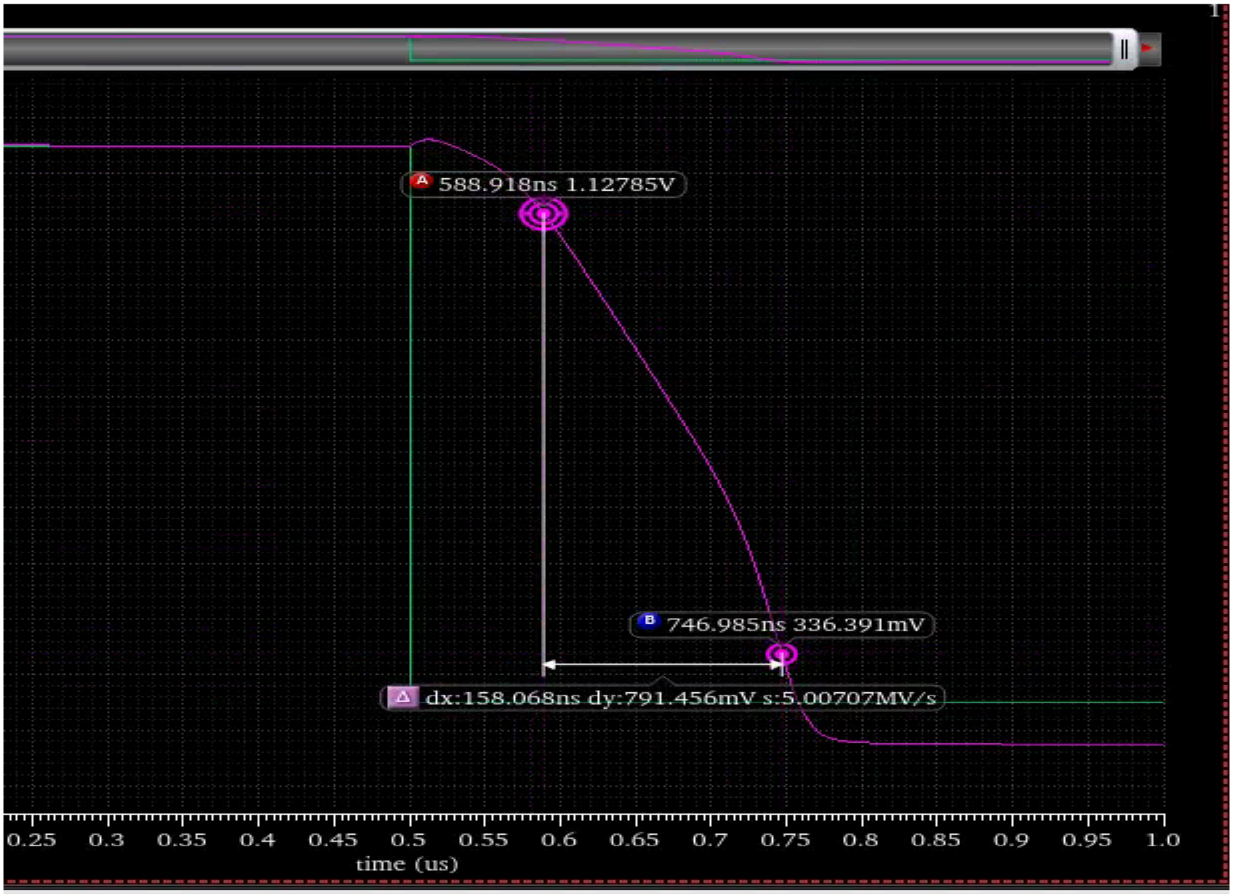

Figure 20. Transient response (fall)

(6.296 + 5.007) / 2 = 5.65

1MV/s = 1V/us

8. Results

The summary of the simulation results is listed below in comparison with the specification of the design.

Specifications	Required	Obtained
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Average Slew Rate (Sr+ + Sr-)/2	>4 V/us	5.65V/us

Figure 1. Table of Design specifications

9. Score

	Avd	OVSR	SR	CMRR	GBW	PM	Pdiss
Simulation Results	76.9608dB	1.217	5.65V/us	70.8598db	6.91MHz	61.197 °	0.087405 mW

Figure 13. Table of Score calculation

$$Score = \min\left[15, 15\left(\frac{Avd}{75dB}\right)\right] + \min\left[15, 15\left(\frac{OVSR}{1.2V}\right)\right] + \min\left[15, 15\left(\frac{SR}{4}\right)\right] + \min\left[10, 10\left(\frac{CMRR}{70dB}\right)\right] + \min\left[15, 15\left(\frac{GBW}{5}\right)\right] + \min\left[15, 15\left(\frac{PM}{60}\right)\right] + \min\left[15, 15\left(\frac{0.1mW}{Pdiss}\right)\right]$$

Figure 14. Score equation

Score = 15+15+15+10+15+15+15= 100

10. Conclusion

A two stage amplifier and single ended output amplifier is designed with an ideal current source and current mirrors. All specifications were met, reaching again of 76.96dB, a unity gain frequency of 6.91MHz, a phase margin of 61.197, and a power dissipation of 0.087mW