EECT/CE 6325 VLSI Design

SAR ADC Logic Controller

Layout & Verification

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The SAR

I chose to design a successive approximation register (SAR) analog-to digital converter controller. A SAR controller operates using a binary search method to determine the value of an analog input signal. It begins by evaluating the most significant bit(MSB), by generating a corresponding digital value that is compared against the voltage stored by the sample-and-hold circuit. Then based on the comparator's result, the controller will either retain or clear the bit and then continue to sequentially search each remaining bit until the least significant bit is resolved.

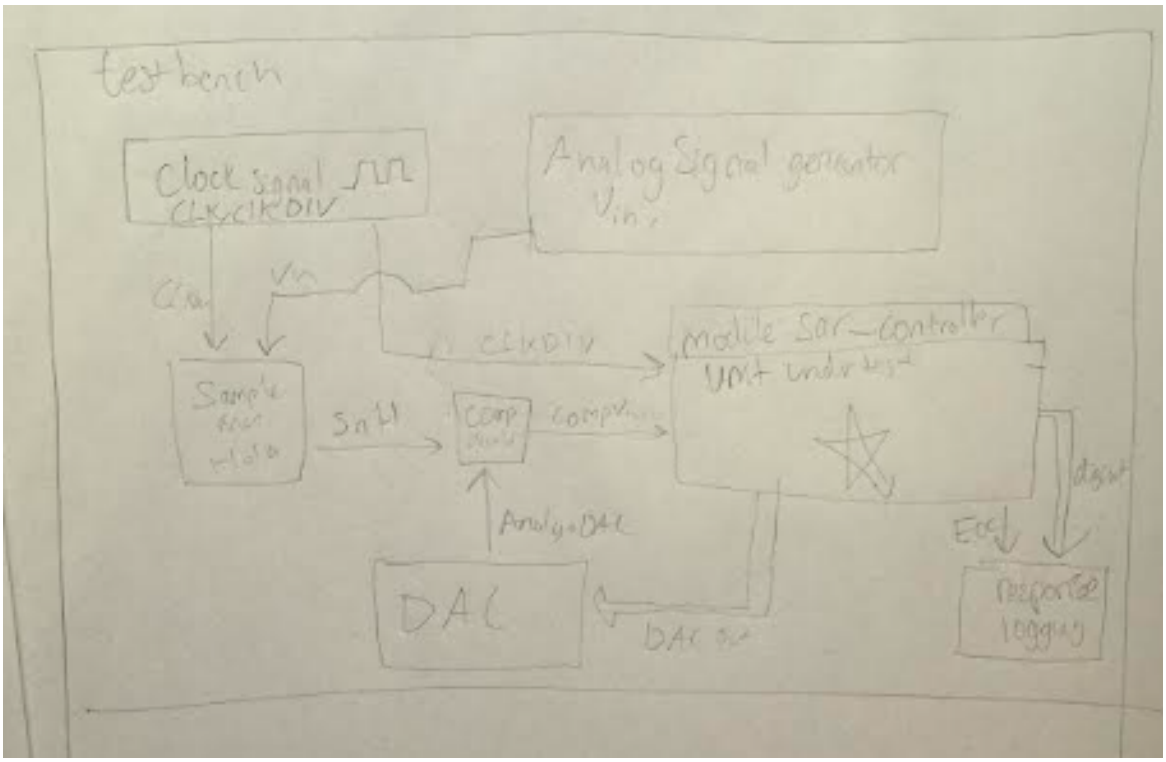

Figure 1 *High level model of a SAR*

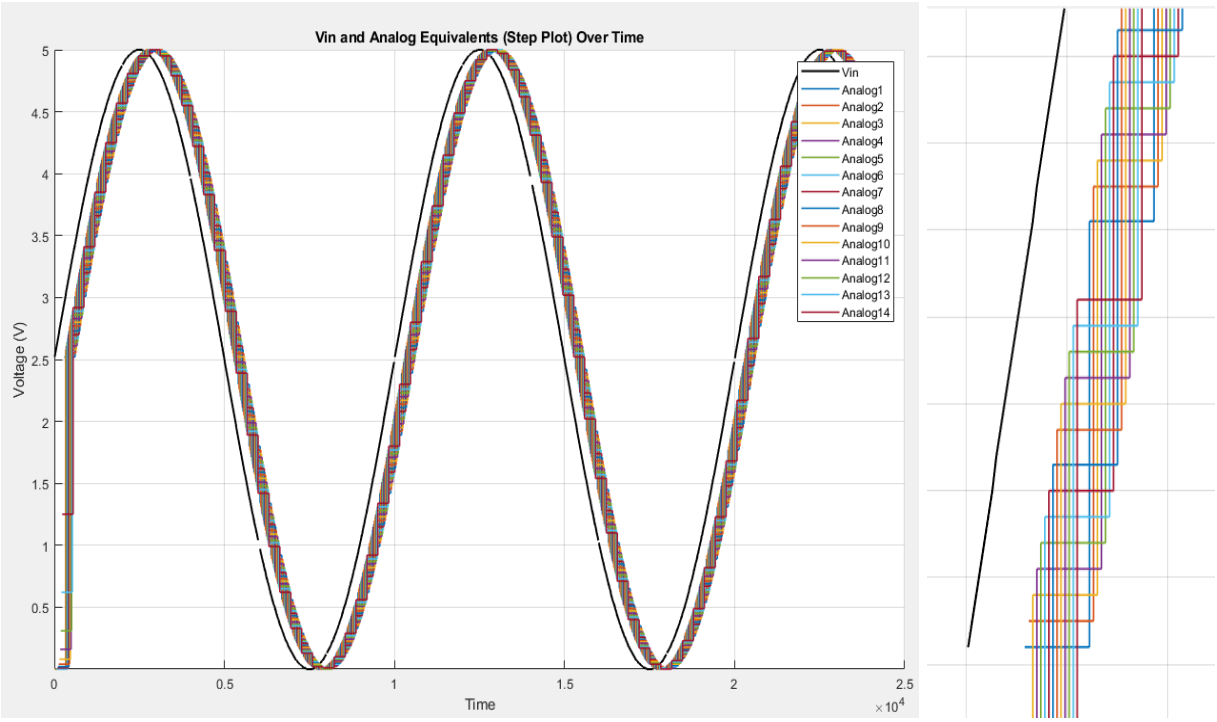

Figure 2 *Testbench verilog results*

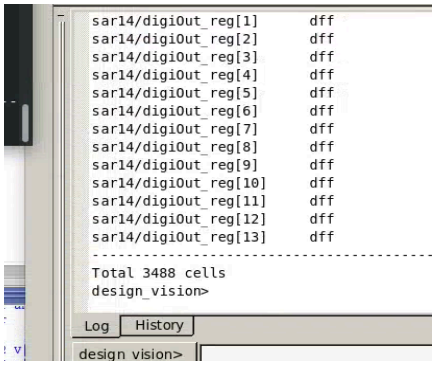

Figure 3 *Cell count*

Design

By reducing overall size we are then able to maximize the number of channels in a given area and allow the design to be scalable with more multi-channel SARs for pipelining implementation which we achieved in the design. Much of my design optimization is derived from space reduction. The standard cells were designed to have a minimum height of 3.38um without the use of horizontal PC layers for connections. A big design challenge was creating a DFF that would match the other standard cells, otherwise we would have to increase the cells of every other cell and therefore increase overall size.

As seen in figure 4,5,6 the design process(and correction) for the DFF to support the quality of the overall design. One of the tradeoffs with an extra inverter is that driving the DFF takes a bit longer so it sacrifices speed, which isn't an issue for most SAR applications.

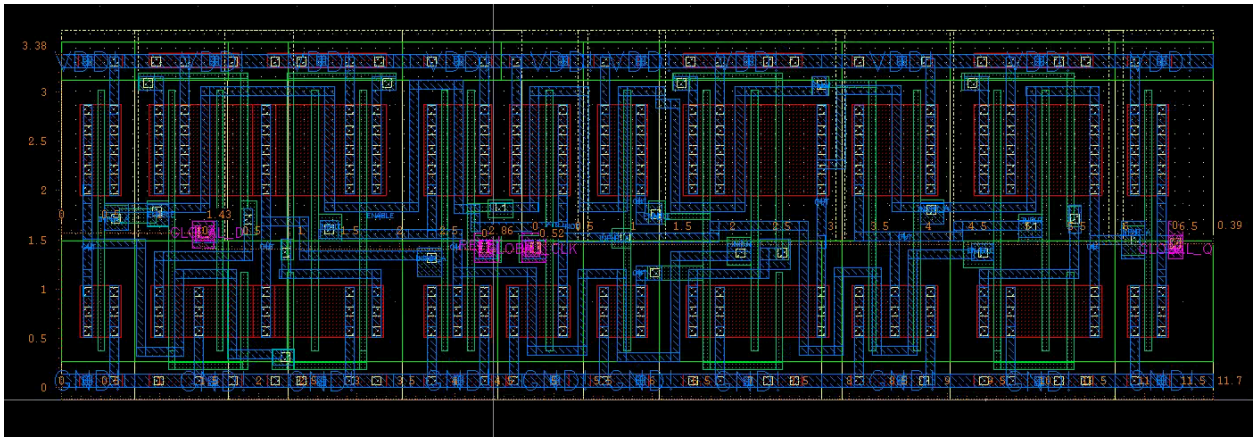

Figure 4 *Fixing*

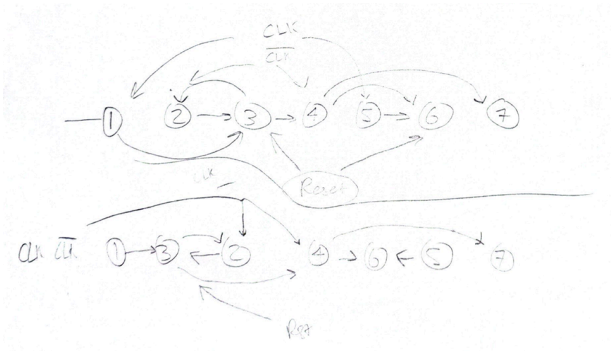

Figure 5 Node Planning

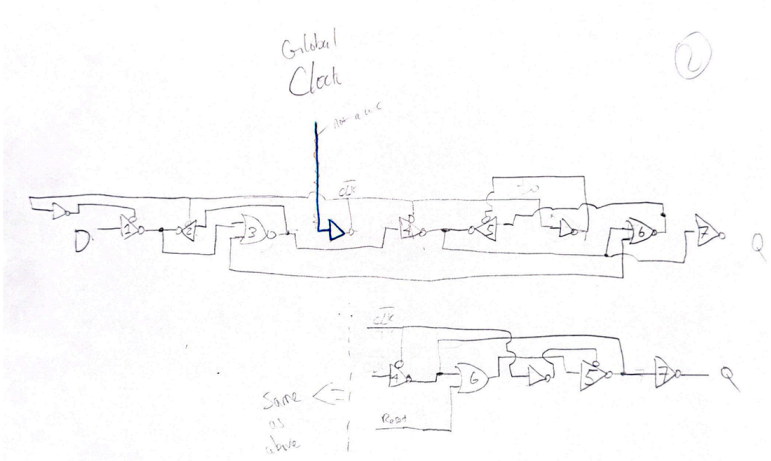

Figure 6 *DFF schematic planning*

Setup Times	(1)	(0)
Tsu_DD	**25 ps**	**6 ps**
Tsu_opt	**41 ps**	**4 ps**
Thold	**6 ps**	**25 ps**
TCLK->Q(optimal)	**329 ps**	**331ps**
tD(optimal)	**370 ps**	**335 ps**
Height	**3.38 um**	-
Width	**11.7 um**	-
Area	**39.546 um^2**	-

Figure 7. DFF Measurements

I noticed PR boundaries weren't automatically set and need to be manually set in the abstract generation step, but correcting it then correctly fit my design for innovus

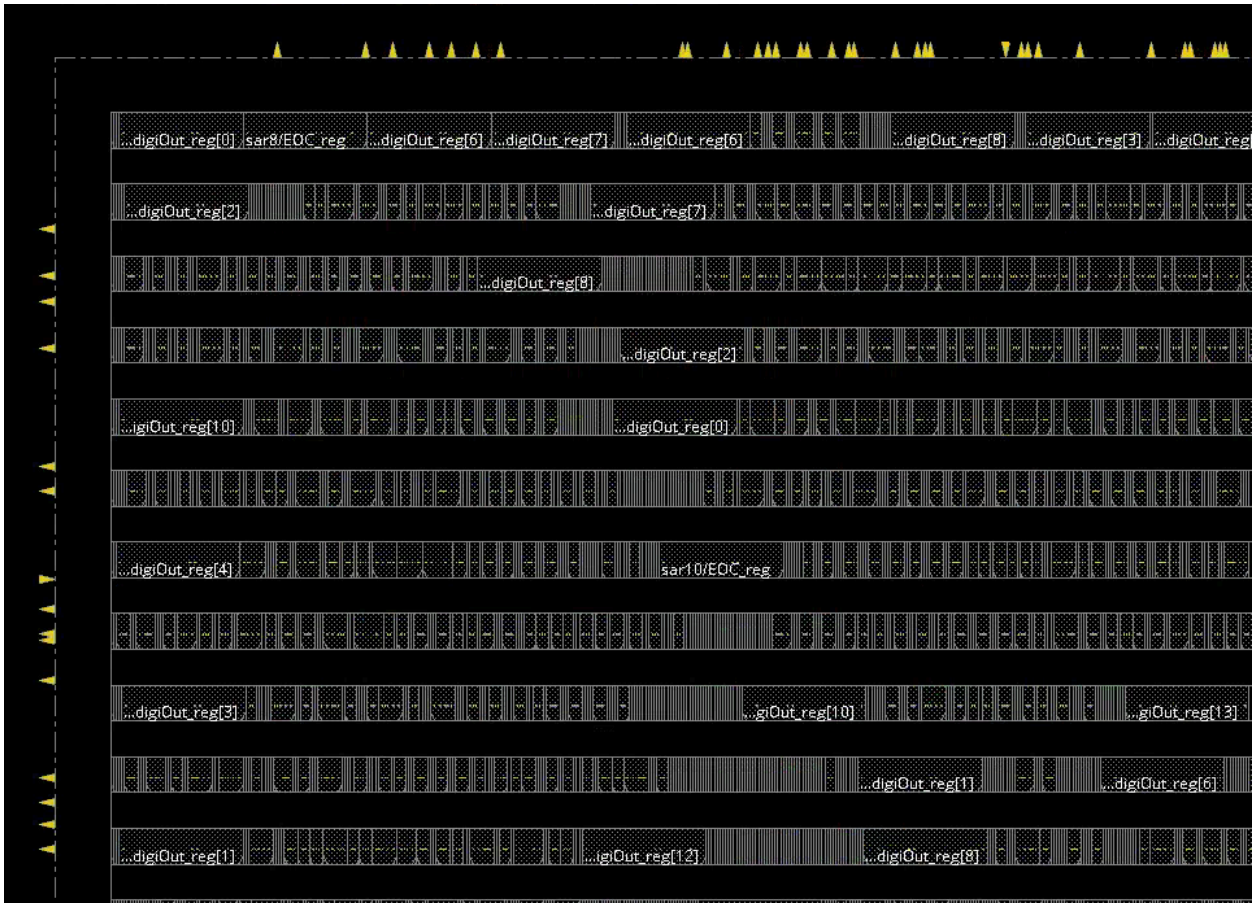

Figure 8 *Standard and Filler placement*

Placement & Routing

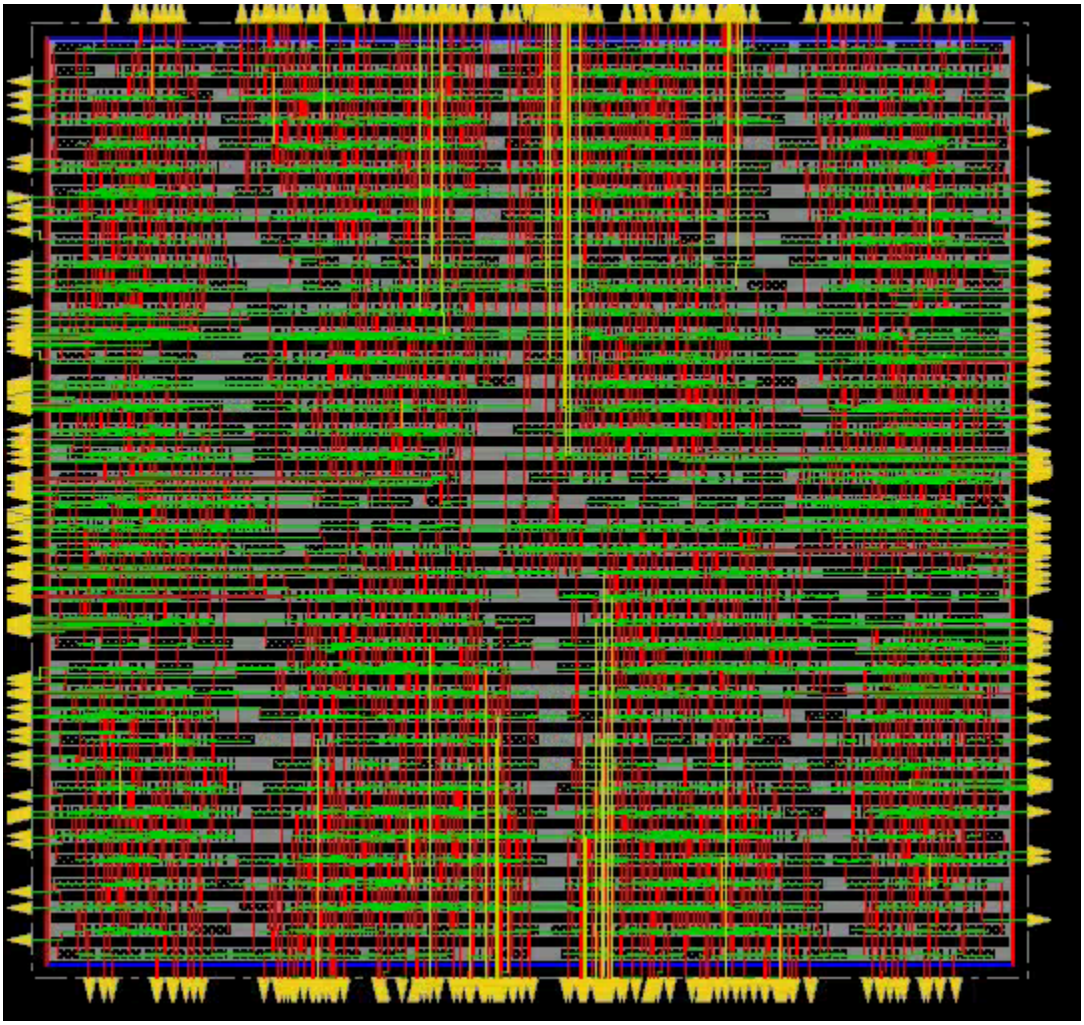

Figure 9. *Innovus routing*

Yes I have that many pins because its a logic unit for multiple channels

```
#CELL_VIEW top_1,init has no DRC violation.
#Total number of DRC violations = 0
#Post Route wire spread is done.
#Total wire length = 75188 um.
#Total half perimeter of net bounding box = 63903 um.
#Total wire length on LAYER M1 = 5712 um.
#Total wire length on LAYER M2 = 39124 um.
#Total wire length on LAYER M3 = 28568 um.
#Total wire length on LAYER M4 = 1308 um.
#Total wire length on LAYER M5 = 477 um.
#Total wire length on LAYER M6 = 0 um.
#Total number of vias = 10598
#Up-Via Summary (total 10598):
#
#-----------------------
# M1                2810
# M2                7691
# M3                  81
# M4                  16
#-----------------------
#                  10598
#
```

Figure 10. Routing report

Then created a design solution by changing outputs by having a width of 0.14 in order to prevent DRC issues

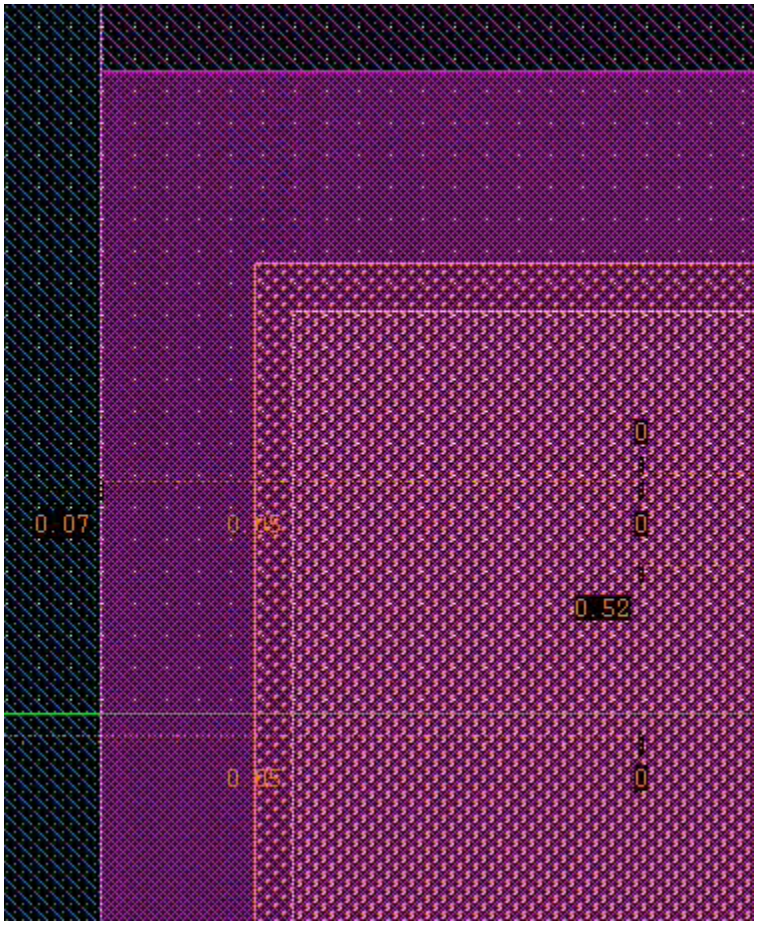

Figure 11. *Noticed using .7 margins about pin center reduced routing errors*

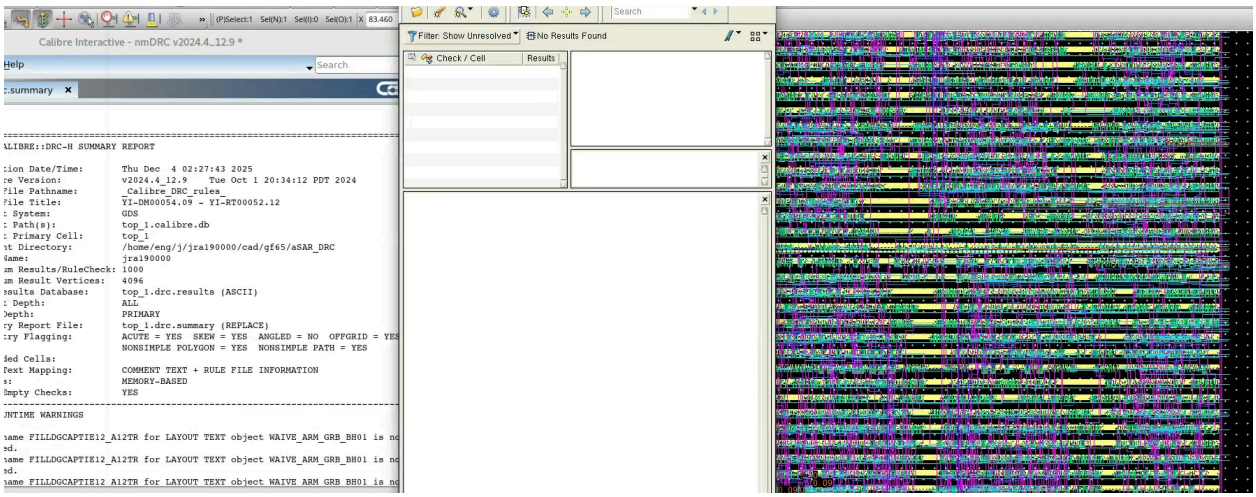

Figure 12 *DRC Check*

Even though I passed through DRC, setting up LVS was a concern because the schematic pins for I also confirmed this works by testing if I included another set of a 2 bit register and saw how it behaved. I switched register names or inputs lvs would not work. It only works when the corresponding output is correctly named (desired effect).

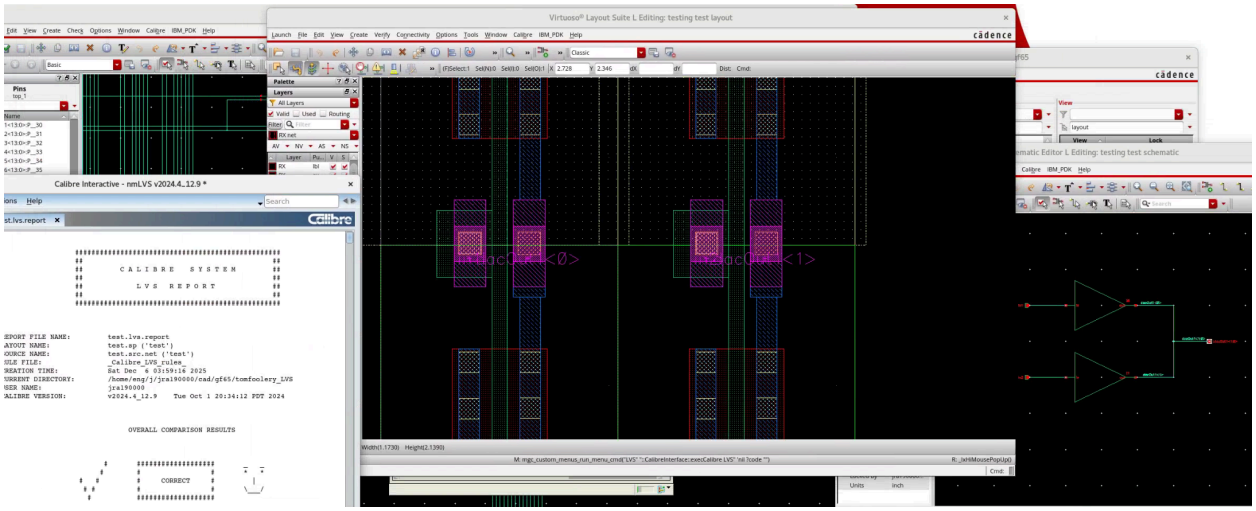

Figure 13 Theory register routing test

Schematic output pin of :DACOUT[0:13] can be referenced as DACOUT<1> or DACOUT<5> as pins in layout. To make LVS work

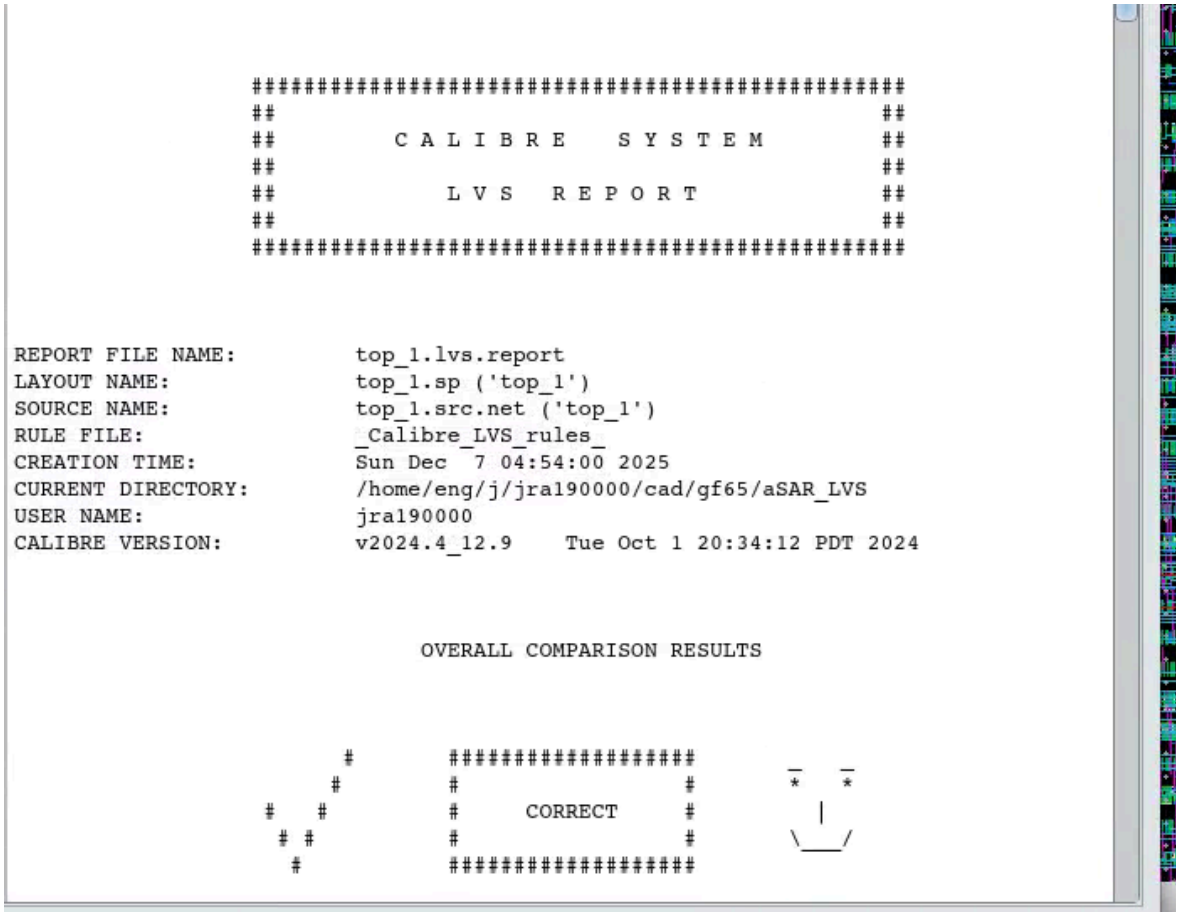

Figure 14. The golden figure: **LVS Check**

H a l l e l u j a h !

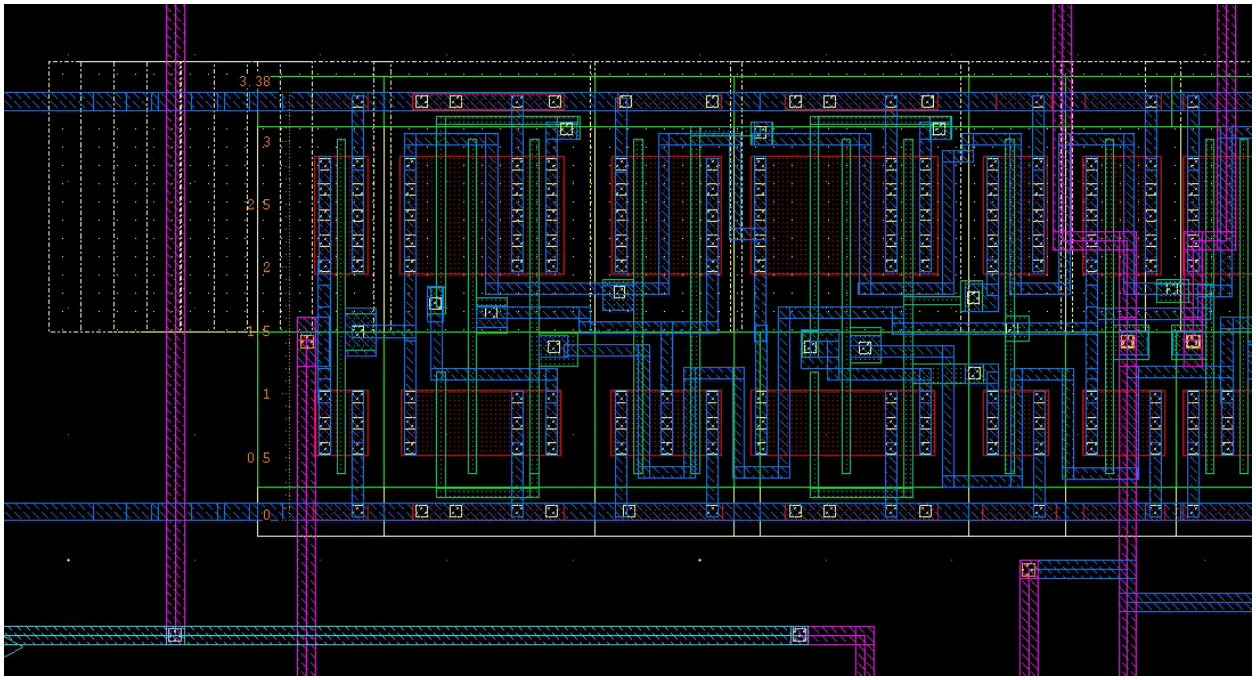

Figure 15. final project 3.38um height check

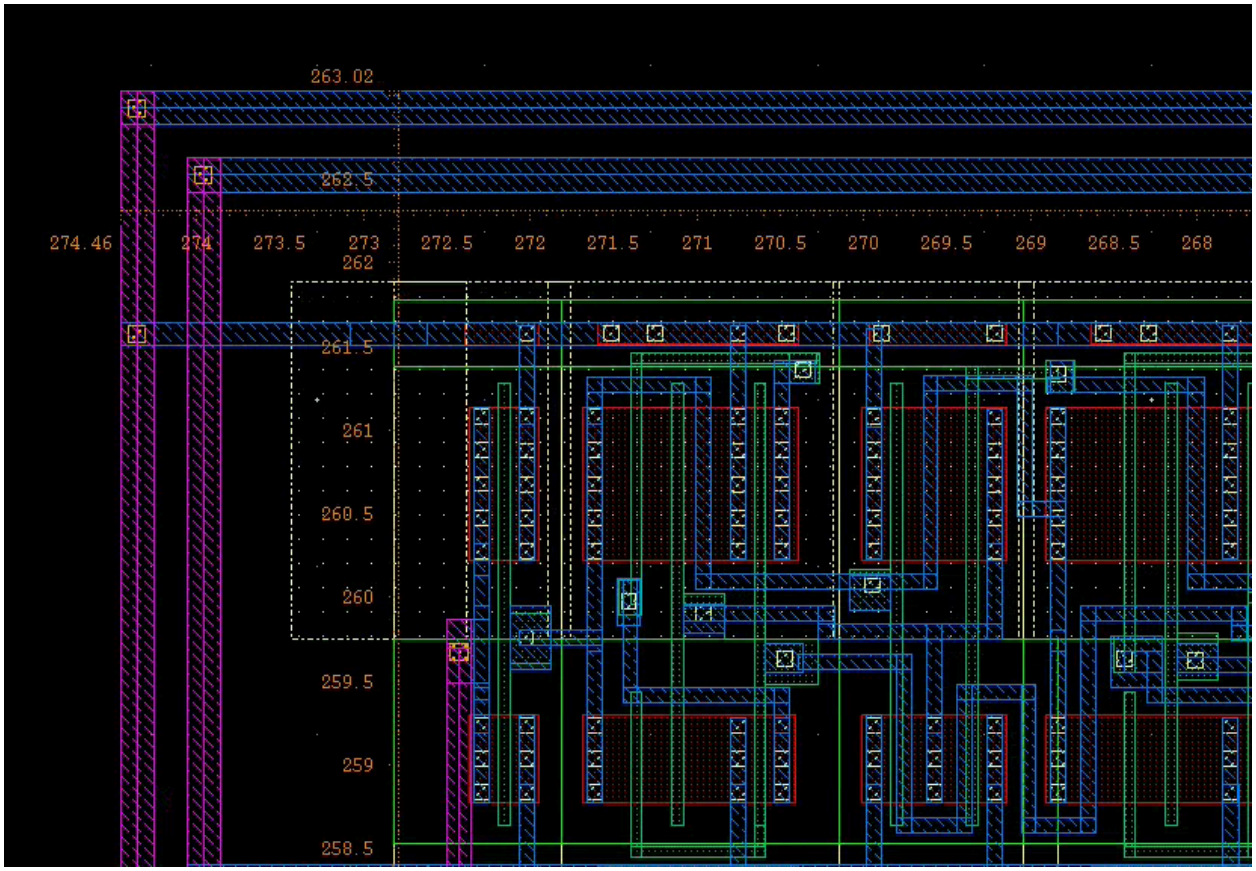

Figure 16 overall size

Conclusion-

This project successfully demonstrates a complete design, layout, and verification of a SAR ADC utilizing a custom library. The final design achieves a compact cell height of 3.38um while maintaining functional correctness and routing feasibility. Additionally, we were able to increase design quality by reducing cell height from design choices. I've learned how to create cells and analyze their characteristics, with this knowledge I will aim to improve cell designs with the context of the final chip demands.