

EECT/CE 7325 VLSI Design

7nm

Cell Design

PROJECT

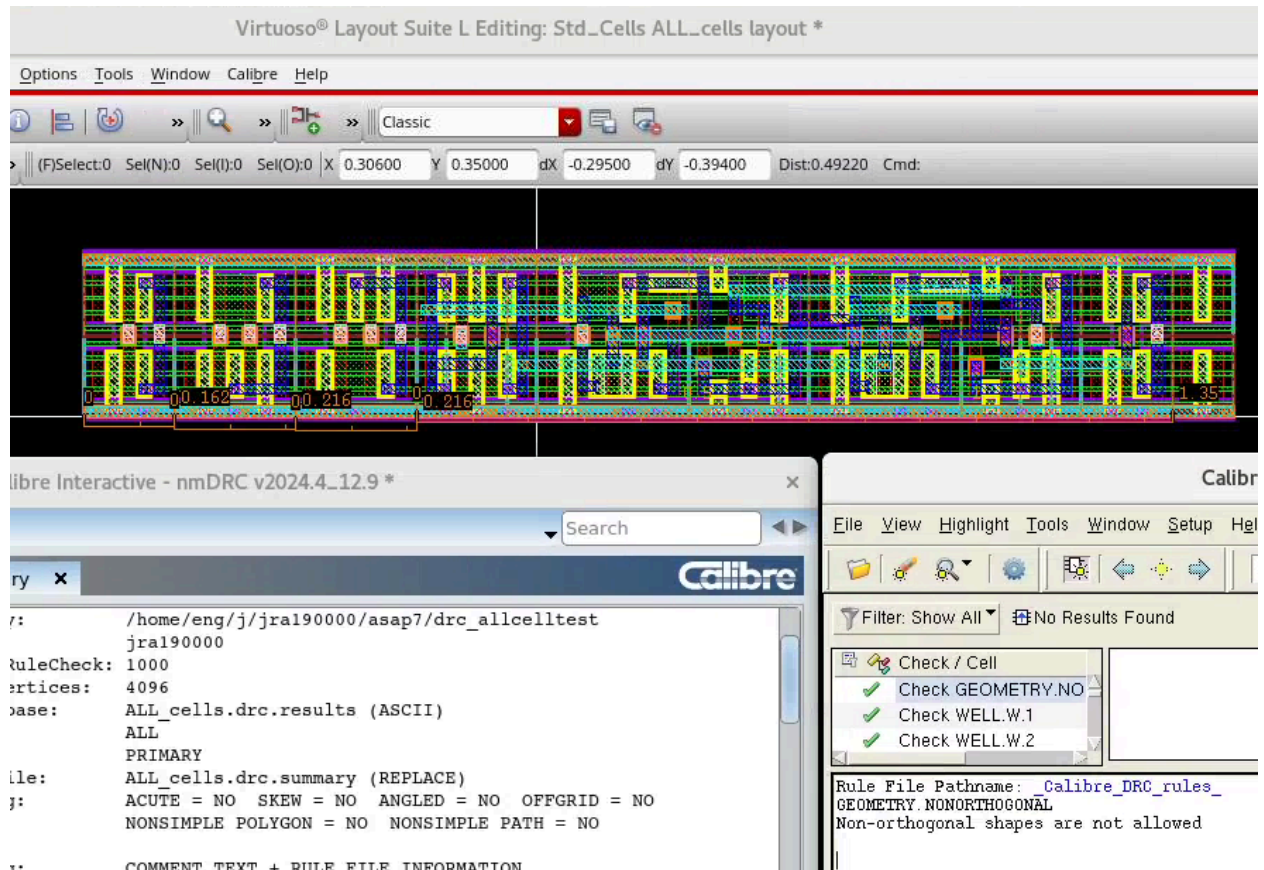
Topic: Verilog/VHDL

Instructor: Sechen

Due Date: Fri. March 28th, 2026

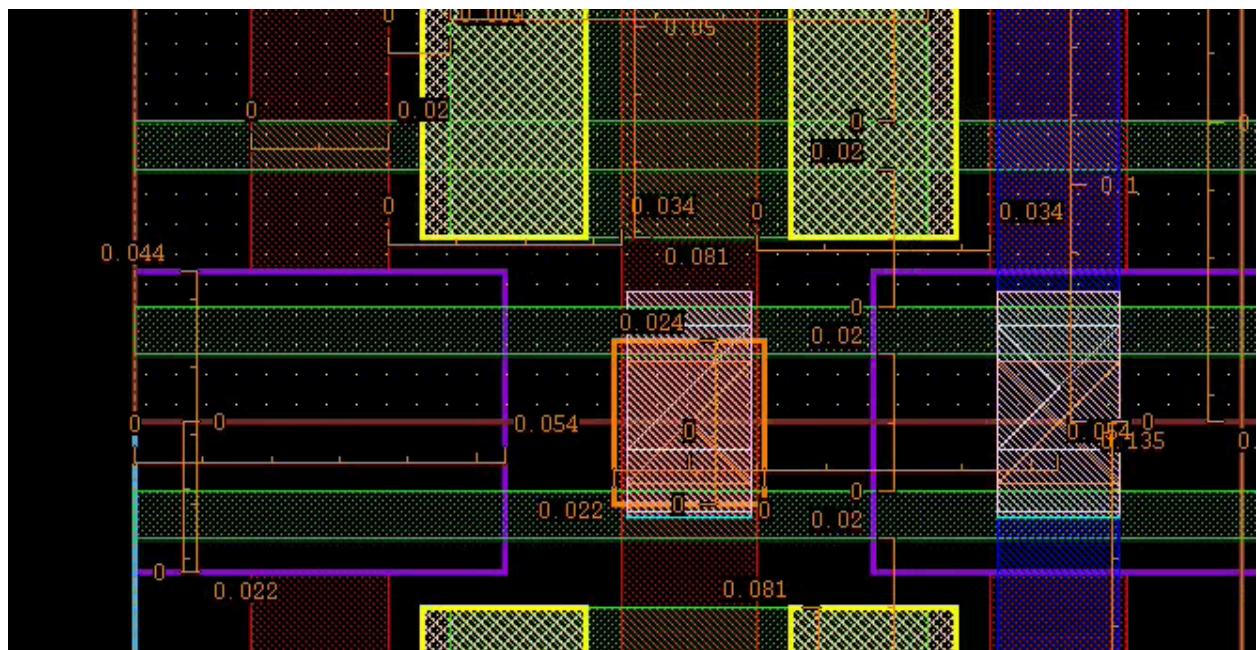
Report Results

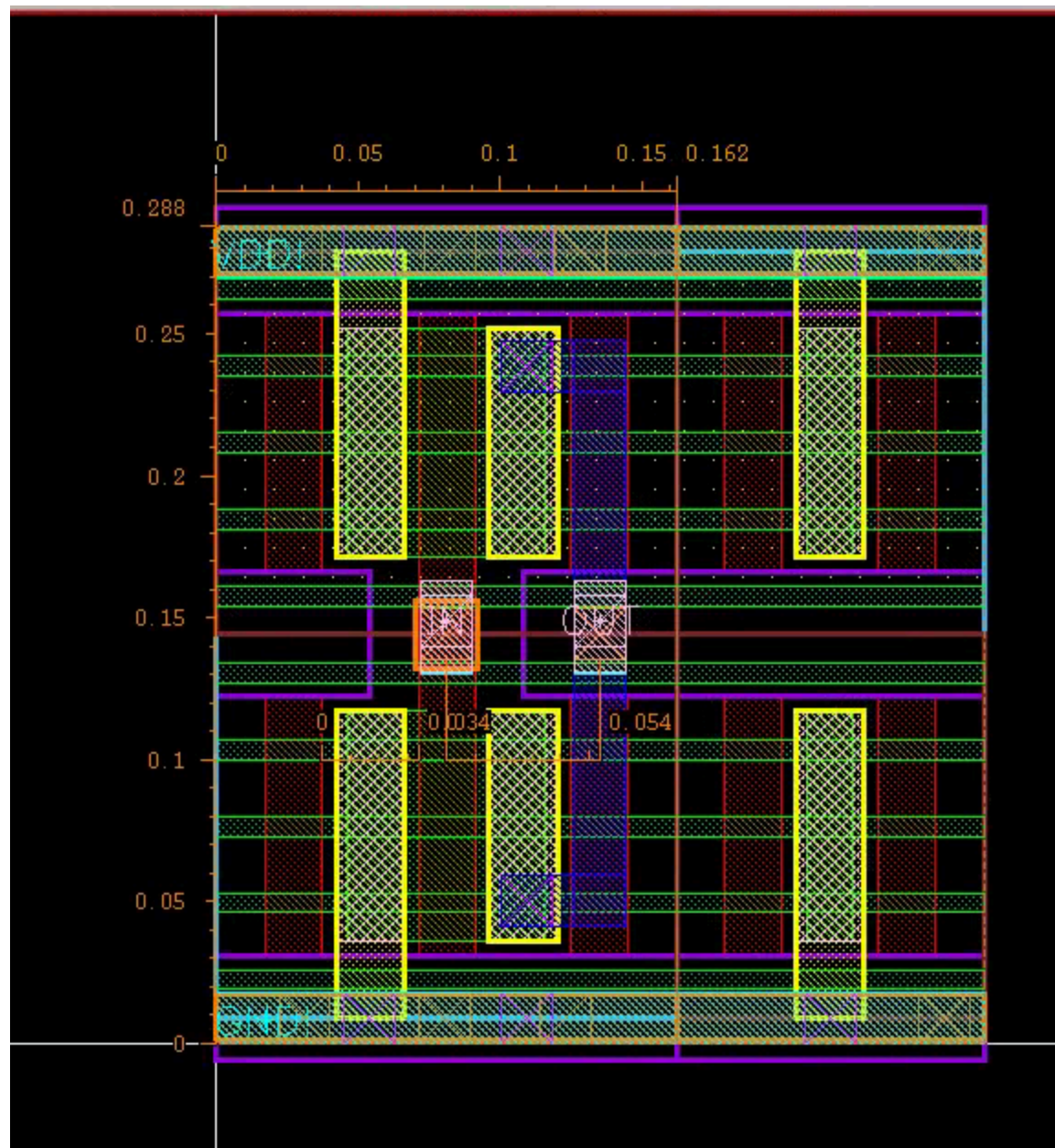
ALL CELLS ON DRC

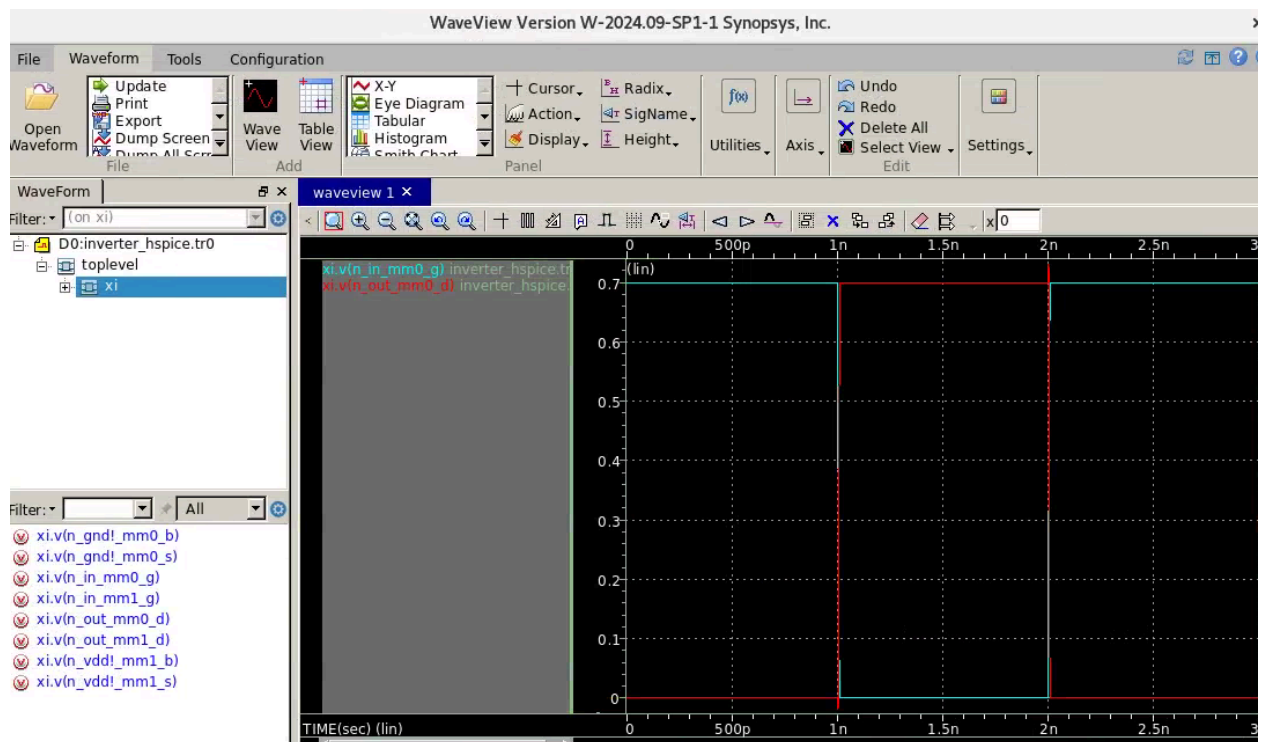
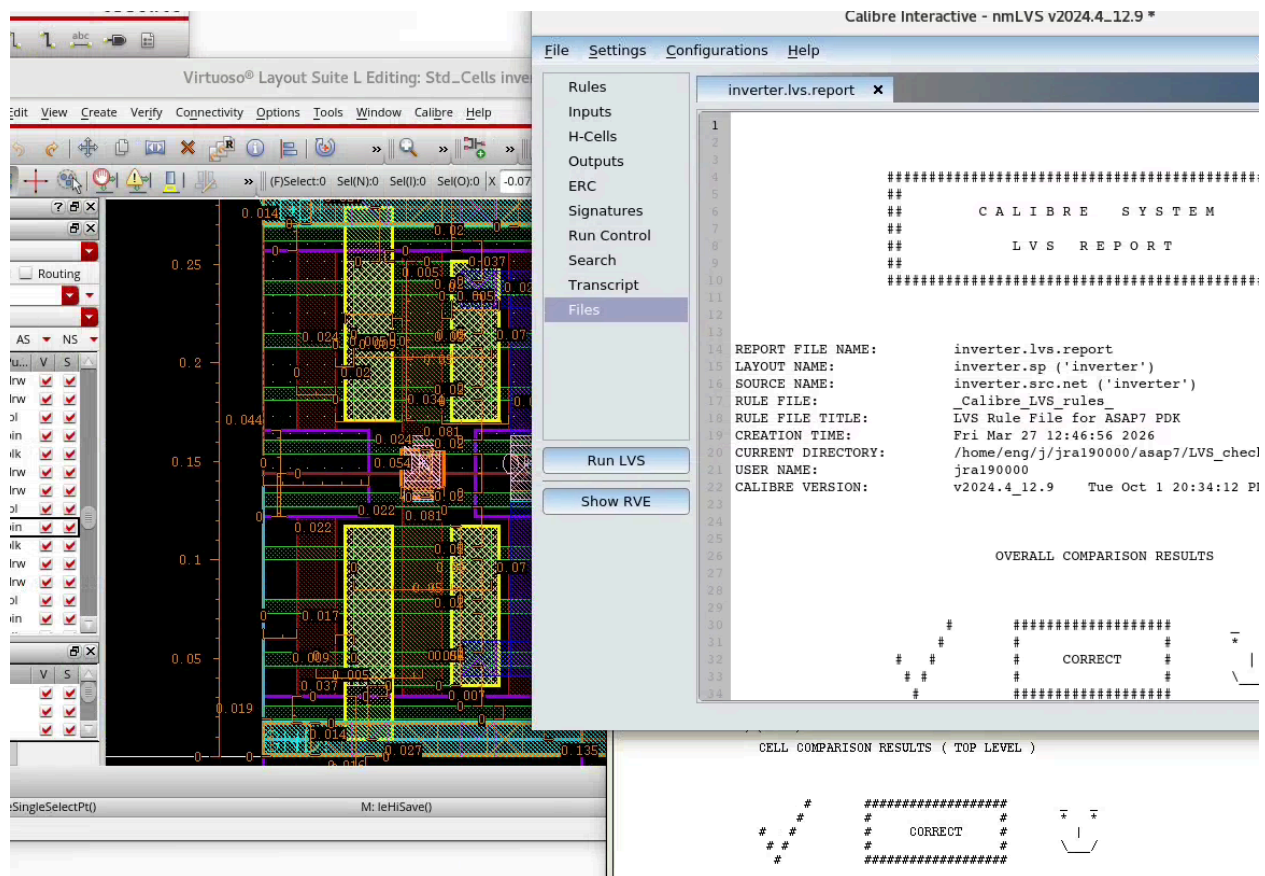


The cells are listed as with dimensions,drc,lvs, and wave form, the .lib file is in zip file inside the synopsys folder named CELLS.lib. Waveforms simulations conducted using 15fG load capacitance, with an input slew rate of 12ps(0-100% and 100-0%). Pdiff and ndiff have 3 fin heights

.288 x .162

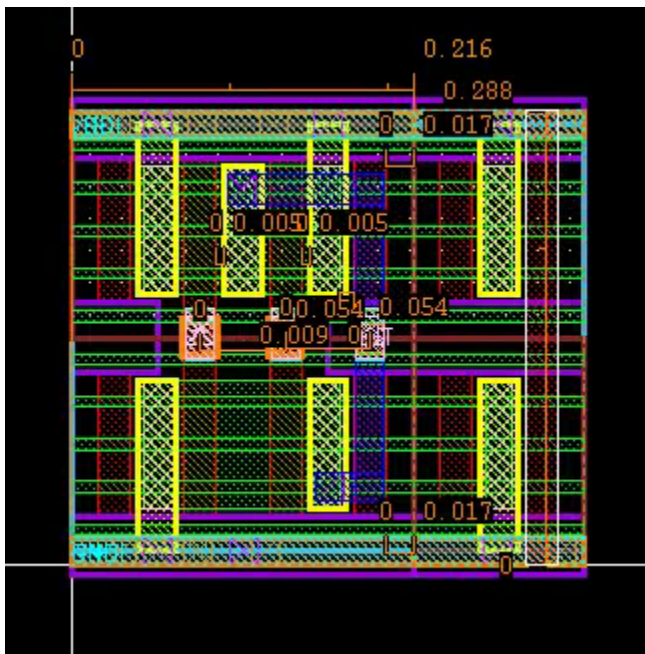
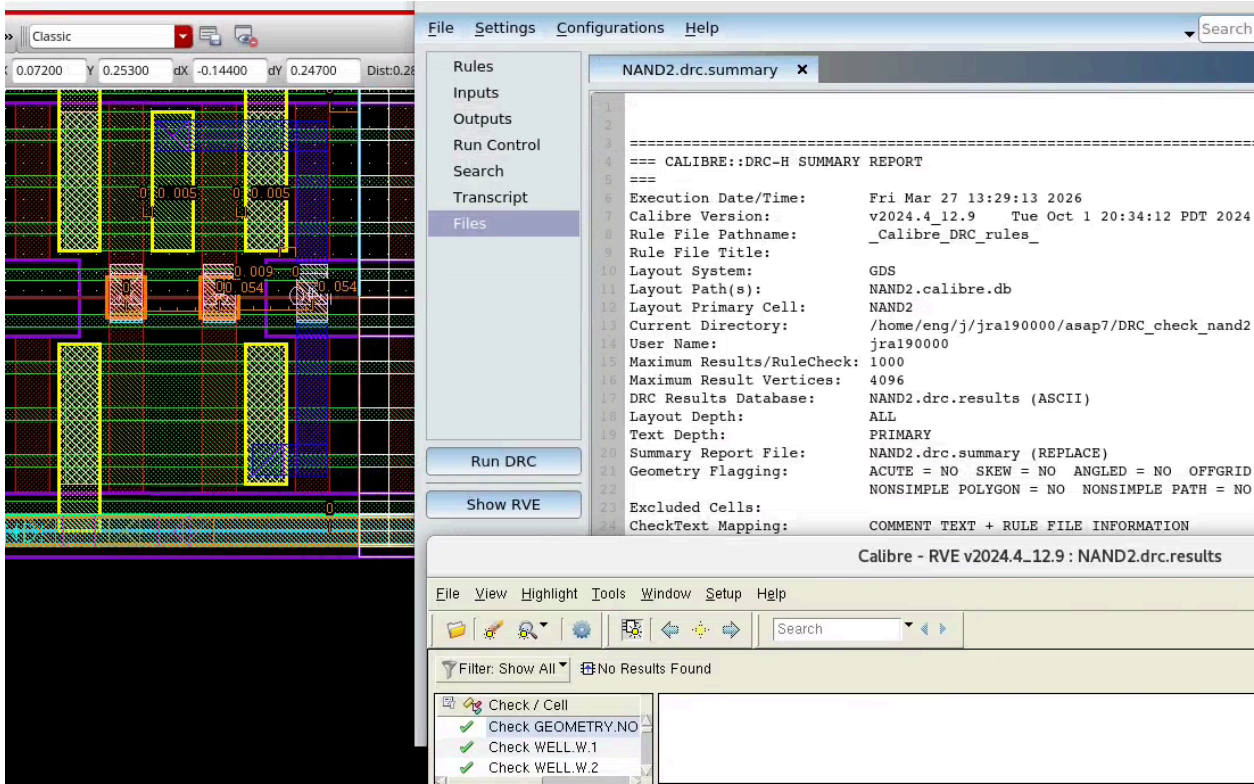




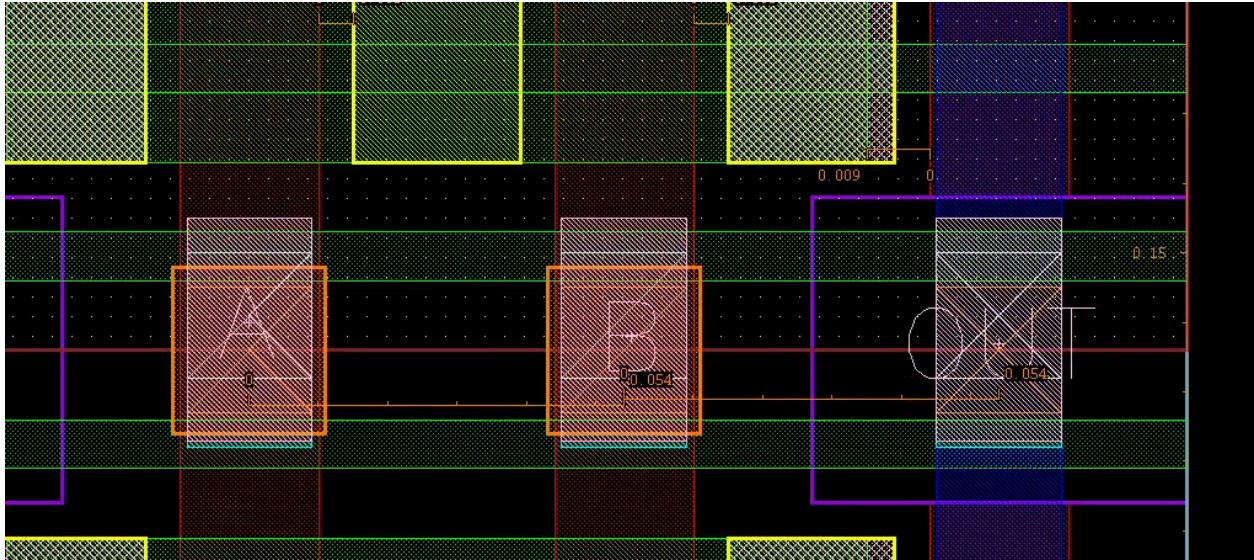


NAND2

.216 x .288



0.216 * 0.288



libre Interactive - nmLVS v2024.4_12.9 *

Search

Calibre

```
#####
##          CALIBRE SYSTEM          ##
##          LVS REPORT              ##
#####

E:      NAND2.lvs.report
      NAND2.sp ('NAND2')
      NAND2.src.net ('NAND2')
      _Calibre_LVS.rules
:      LVS Rule File for ASAP7 PDK
      Fri Mar 27 13:46:14 2026
RY:    /home/eng/j/jral90000/asap7/LVS_check_nand2
      jral90000
:      v2024.4_12.9    Tue Oct 1 20:34:12 PDT 2024

OVERALL COMPARISON RESULTS

#          #####
#          # CORRECT #
#          #          #
#          #####
```

Comparison Results x

Layout Cell / Type

Source Cell

NAND2

NAND2

Cell NAND2 Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVE

#

CORRECT

#

INITIAL NUMBERS OF OBJECTS

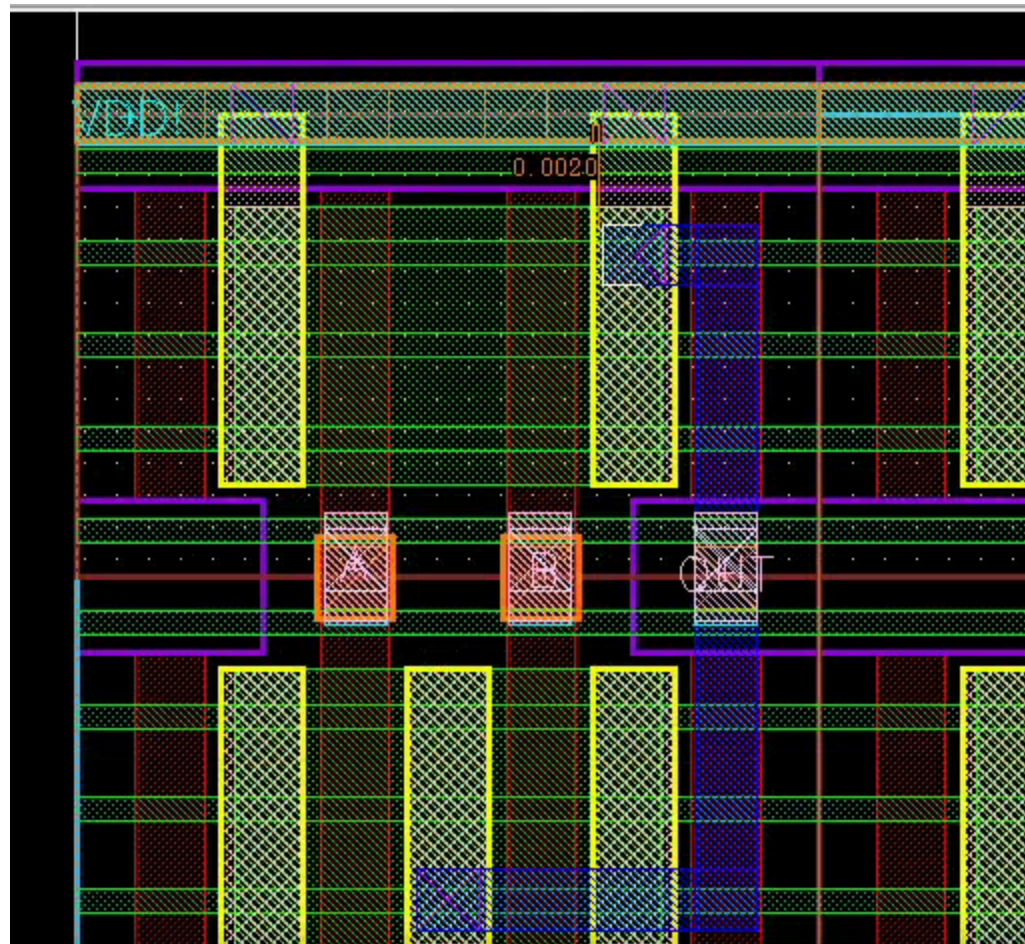
Layout Source Component Ty

Ports: 5 5

Nets: 6 6

Instances: 0 0

WY / A nins



Calibre - RVE v2024.4.1

View Highlight Tools Window Setup Help

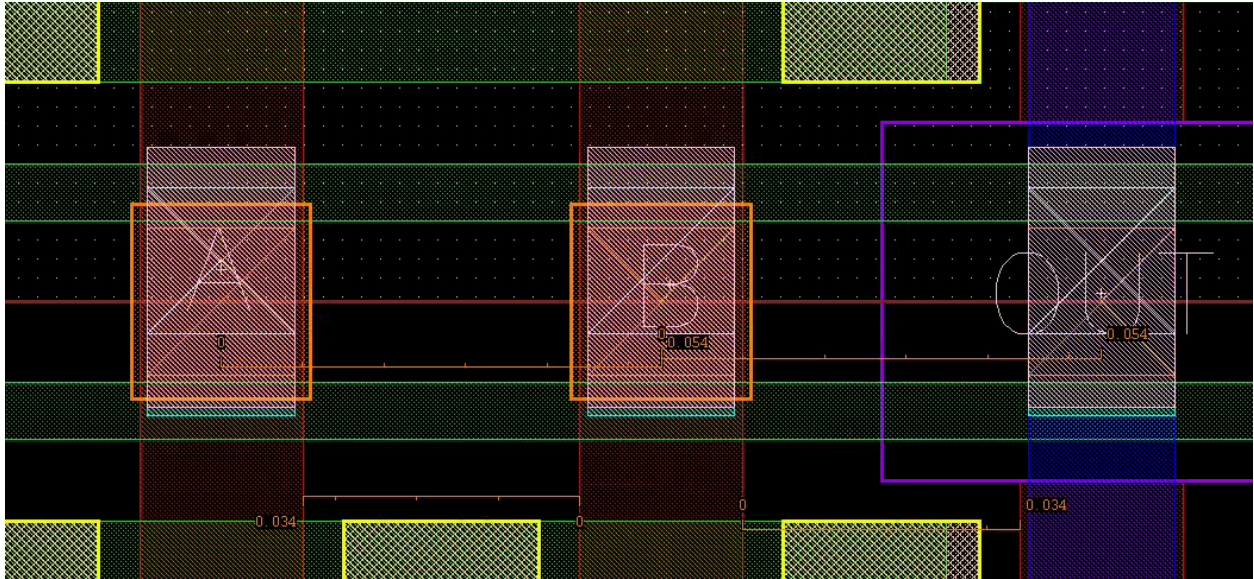


Filter: Show All No Results Found

- Check / Cell
- Check GEOMETRY.NO
- Check WELL.W.1
- Check WELL.W.2

File Pathname: _Calibre_DRC_rules_
ENTRY.NONORTHOGONAL
orthogonal shapes are not allowed

drc



ve - nmLVS v2024.4_12.9 *

Search

Calibre

CALIBRE SYSTEM
LVS REPORT
#####

OR2.lvs.report
OR2.sp ('NOR2')
OR2.src.net ('NOR2')
Calibre_LVS_rules_
VS Rule File for ASAP7 PDK
ri Mar 27 14:04:36 2026
home/eng/j/jral90000/asap7/LVS_check_nor2
ral90000
2024.4_12.9 Tue Oct 1 20:34:12 PDT 2024

OVERALL COMPARISON RESULTS

CORRECT #
#####

0.034

0.054

0.054

0.034

0.0020

M: leHISave()

File View Highlight Tools Window Setup Help

Comparison Results x

Layout Cell / Type | Source Cell

NOR2 | NOR2

Cell NOR2 Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL

CORRECT #
#####

LAYOUT CELL NAME: NOR2
SOURCE CELL NAME: NOR2

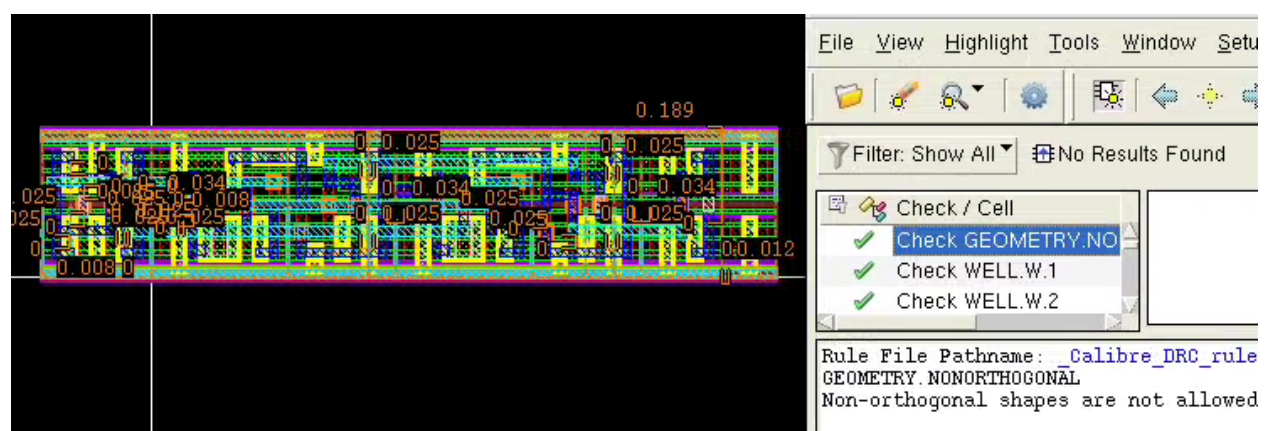
INITIAL NUMBERS OF OBJECTS

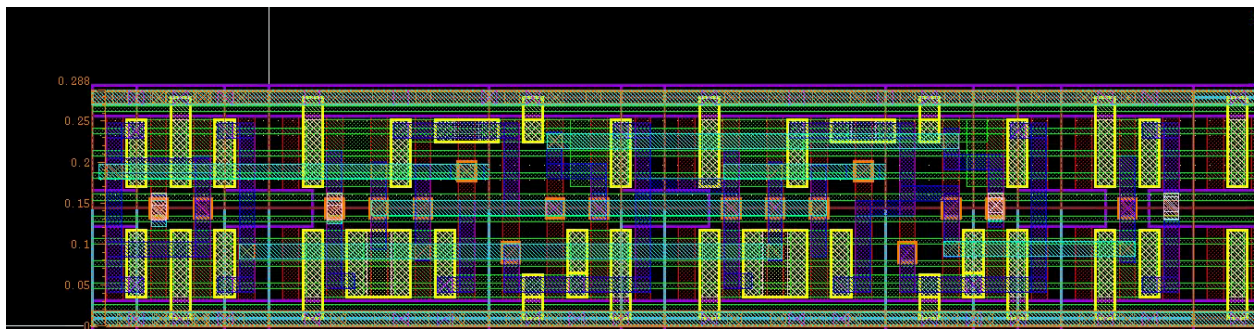
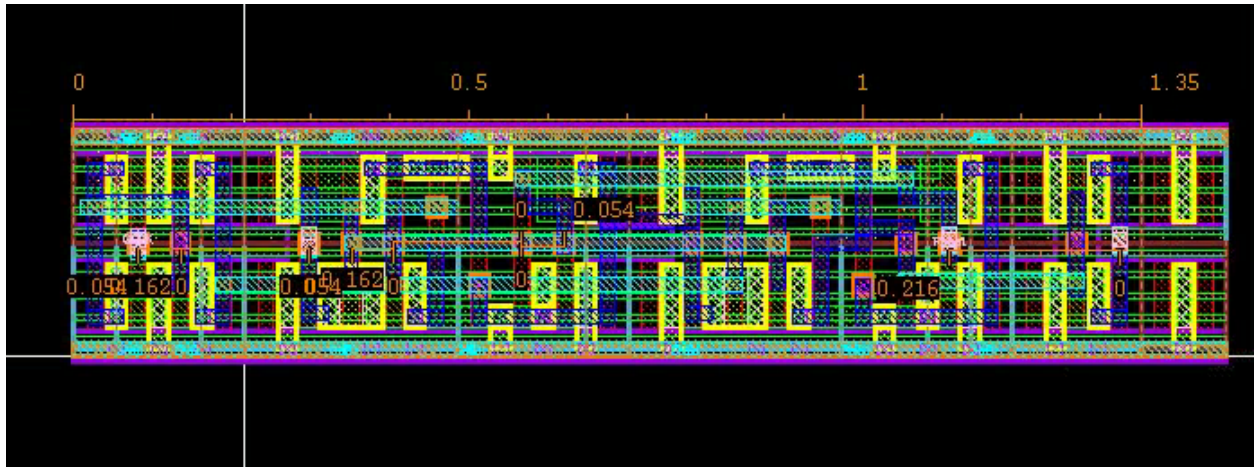
	Layout	Source	Component Typ
Ports:	5	5	
Nets:	6	6	

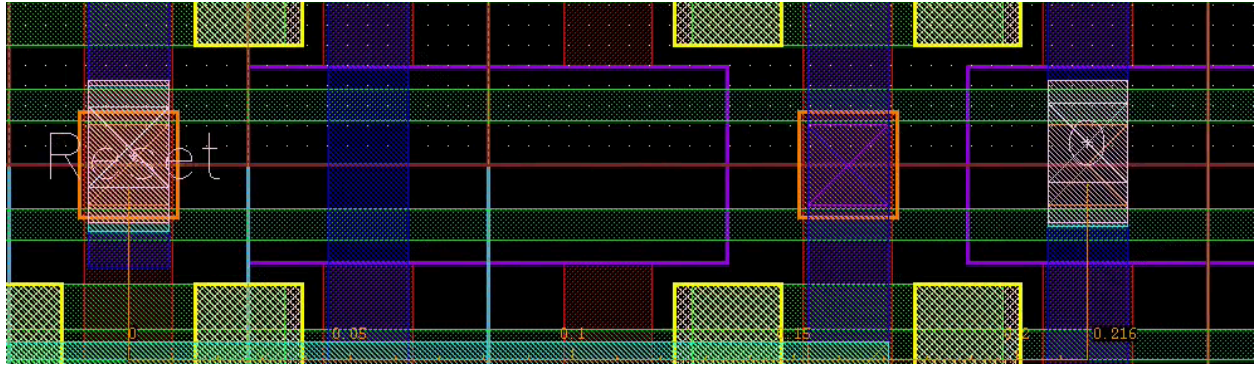
lvs

 1.35×0.288

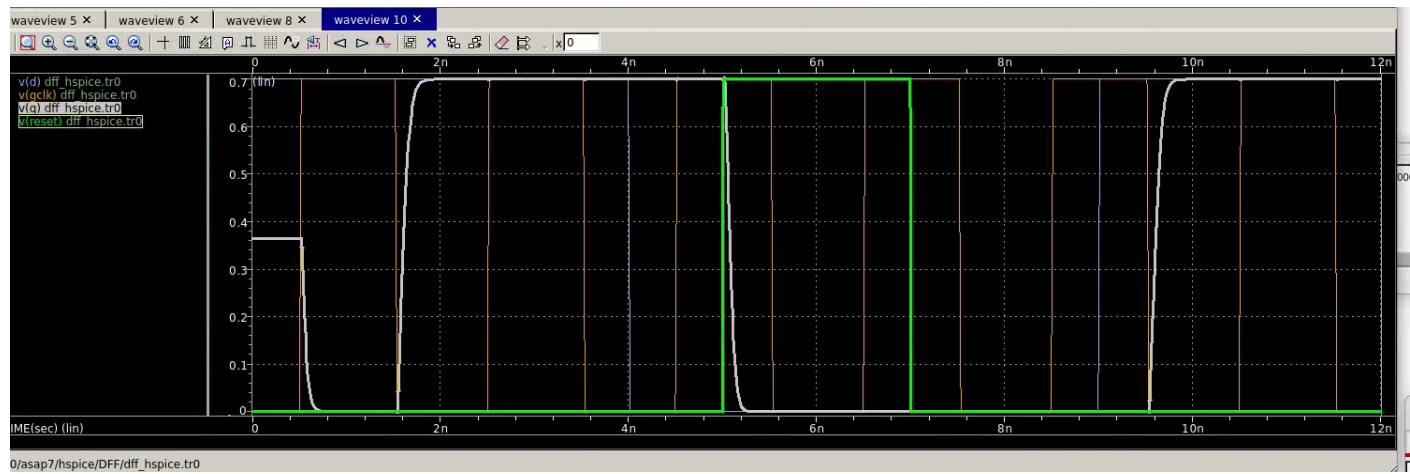
drc







Currently have 3 diffusion breaks. I could have made it better if I flipped horizontally the first latch portion to eliminate a diffusion break. Didn't realize how the DRC rules for active region margin for excised gates worked, until after I finished the DFF. but could rewire m2 rails to allow for only two diffusion breaks. This works as neg edge dff.



.lib file is included in zipfile

ALL CELLS ON DRC

