

Justin Alejandro

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Education

University of Texas at Dallas, Richardson, Texas

Master of Science in Electrical Engineering, *MSEE* (Dec 2026)

GPA: 3.9/4.0

Bachelor of Science in Electrical Engineering, *BSEE* (May 2024)

Relevant Course Work: Advanced VLSI Design, VLSI, ASIC Design, HDL Modeling, Analog IC Design, RF & Microwave Circuits

Skills

Languages & HDL: Verilog, C/C++, Tcl, MATLAB/Simulink

EDA & Tools: Cadence Virtuoso, Cadence Genus, Cadence Innovus, Synopsys Design Vision, Synopsys PrimeTime, HSPICE, ModelSim, Waveview

Work Experience

Texas Instruments -- Sugarland, TX

May 2026 – Aug 2026

Applications Engineering Intern

- Engineered an AI-assisted C2000 MCU code-generation framework by parsing TI SDK source and examples into structured Markdown context for agents in Code Composer Studio integration, reducing MCU configuration development time from 3 weeks to 3 days (~86%).
- Ported and validated real-time AC/DC and DC/DC digital power control for an onboard charger reference design (TIDM-02013) from F28x to F29x, achieving functional hardware operation and verifying high resolution PWM waveforms, Trip Zone protection, and safety ISRs.

University of Texas at Dallas -- Richardson, TX

Jan 2024 – Jul 2025

Signals & Systems Research Engineer

- Designed a novel geolocation algorithm, leveraging a modifying version of Dijkstra's algorithm to optimize path finding across network topologies; resulted in a published paper & patented invention for efficient geolocation solutions.
- Collaborated with a cross-disciplined, international team in medical and software development fields such as the National Institute of Health (NIH) to create geolocation solutions in Uganda study. Research has now progressed to collaborate in search case studies with police and parks.

Mouser Electronics, -- Mansfield, TX

Jun 2022 - Aug 2022

Applications Engineering Intern

- Designed and prototyped an automated air ventilation system using I²C and UART for sensor integration and motor control.
- Researched and tested application use-cases for semiconductor supplier products, documenting performance and feasibility.

Projects

Low Power Mini Stereo Digital Audio Processor | Verilog, Tcl scripting | ASIC design

Spring 2026

- Software/ Hardware codesign of a dual channel digital audio DSP ASIC using optimized chip design to perform a customized multiplier-less PoT convolution algorithm in Verilog, implementing ALU datapaths, FSM control, CDC synchronizers, and multi-channel SRAM memory architecture on the 7nm ASAP PDK using standard cell-based design. Scripting flow automation in Tcl.
- Executed the complete RTL-to-GDSII ASIC flow using ModelSim, Design Vision, Cadence Genus and Innovus, including synthesis, floor planning, SRAM macro integration, power-grid design, place-and-route, STA timing closure, and physical optimization.
- Performed post-layout verification and PPA analysis, achieving 19,757um² area, 0.151mW power, and 640MHz frequency.

Successive Approximation Analog-to-Digital Controller (SAR ADC) | Global Foundries 65nm | Physical design & VLSI

Fall 2025

- Designed and implemented a 16-bit SAR ADC controller in Verilog, coordinating DAC trial-bit sequencing, comparator input capture, and end-of-conversion logic, with a multi-channel pipeline architecture for increased throughput; verified functional correctness via test bench simulation in ModelSim.
- Synthesized the RTL into a gate-level netlist in Design Vision and built full custom standard cells from schematic to layout in Cadence Virtuoso, characterizing cell timing and power in HSPICE — generating Liberty (.lib) models and performing waveform-level analysis in Waveview.
- Placed and routed a 3,200-cell physical design in Cadence Innovus, ran static timing analysis (STA) in PrimeTime for timing closure, and performed DRC and LVS physical verification to confirm layout integrity.

7nm FinFET Physical Design - 128b Serial-to-Parallel Converter | Verilog, Cadence | Physical Layout & VLSI

Spring 2026

- Designed a 128-bit serial-to-parallel conversion architecture in Verilog and verified functional correctness via testbench simulation in ModelSim.
- Synthesized the RTL into a gate-level netlist in Design Vision and built a full custom cell library from schematic to layout in Cadence Virtuoso on the 7nm ASAP FinFET PDK, characterizing cells in HSPICE and generating Liberty (.lib) timing/power models.
- Hand-performed manual place-and-route and custom floorplanning for the 700-cell physical design in Virtuoso — without EDA automation — and verified layout integrity through DRC and LVS physical verification.

TSMC 16nm Advanced VLSI Independent Study | Cadence | Physical design & VLSI

(Ongoing) Fall 2026

- Conducting independent research under Dr. Carl Sechen to design and physically implement digital integrated circuits on TSMC 16nm and ASAP 7nm FinFET fabrication processes alongside Ph.D. students.
- Developing FP8 MAC unit optimization using CLA and CSA techniques in tandem with Wallace tree multipliers to improve area, power, and timing.

Custom Differential Amplifier | Cadence Virtuoso | Analog IC Design

Fall 2026

- Designed a two-stage differential amplifier using current mirrors and Miller compensation at 1.5V supply with a 2pF load, achieving 76.96dB voltage gain, 70.859dB CMRR, 6.91MHz unity-gain frequency, 61.19 degrees phase margin, and 0.0874mW power dissipation.

Publications

I-NAV: Inverse Navigation for questionnaire-based geolocation in GPS-denied environments, Array, Volume 31, 2026, 100978, ISSN 2590-0056,

Sep 2026

Developed a novel geolocation machine learning algorithm from the ground up, modifying Dijkstra's algorithm to generate isochrones for improved positioning in GPS-denied environments. <https://doi.org/10.1016/j.array.2026.100978>